



Fragmentation to Scalability: A Unified Automation and AI Stack for Multi-Die Design

EDPS 2026

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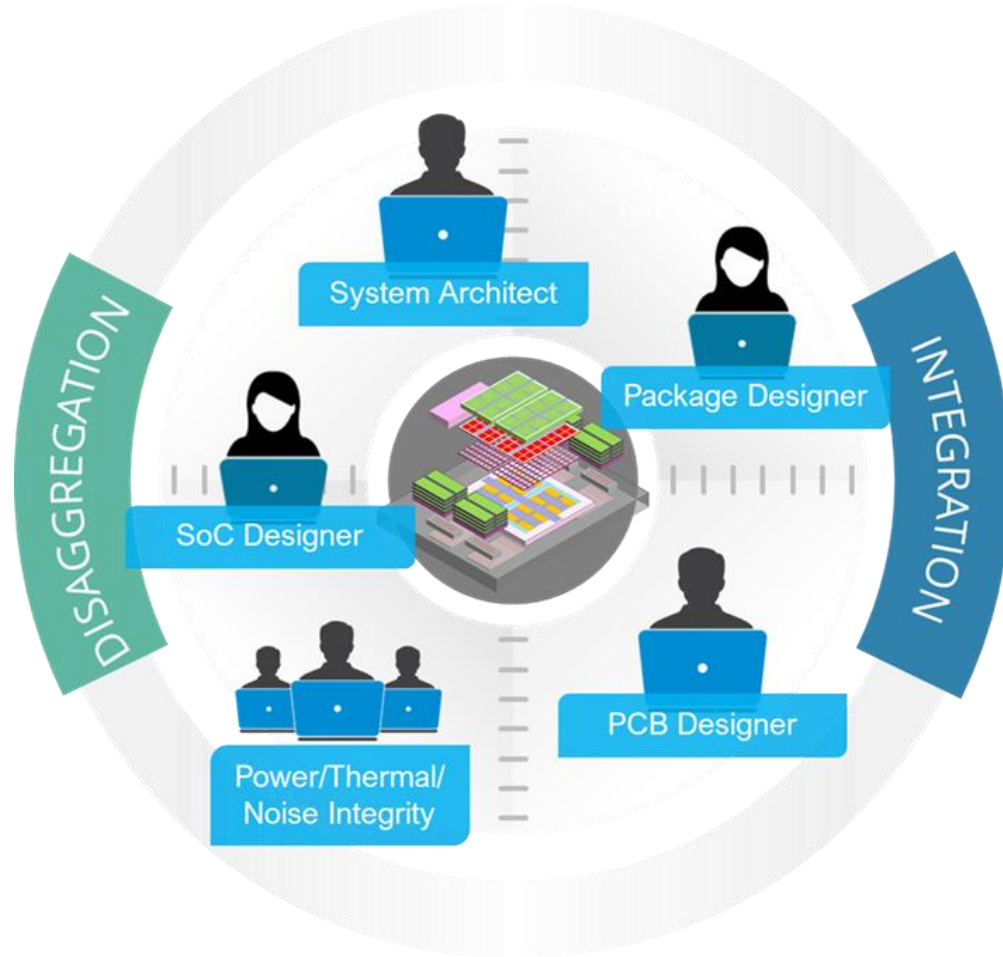
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The Heterogeneous Integration Design Process

Integration of Chiplets Also Implies Integration of Workflows

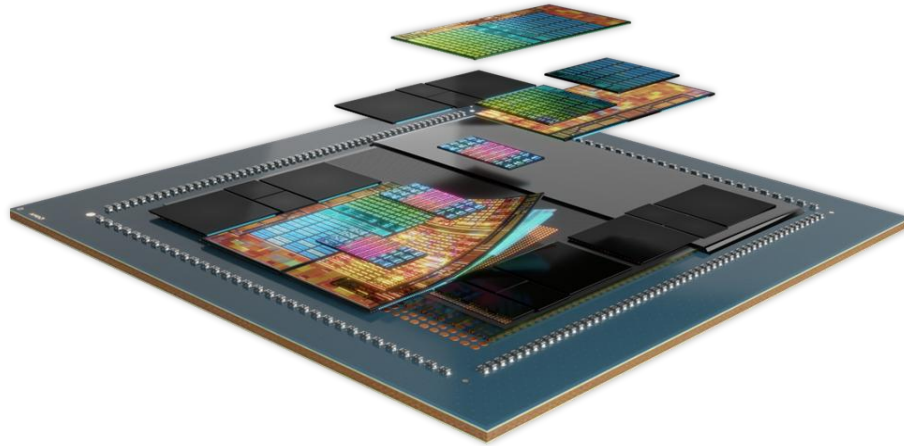
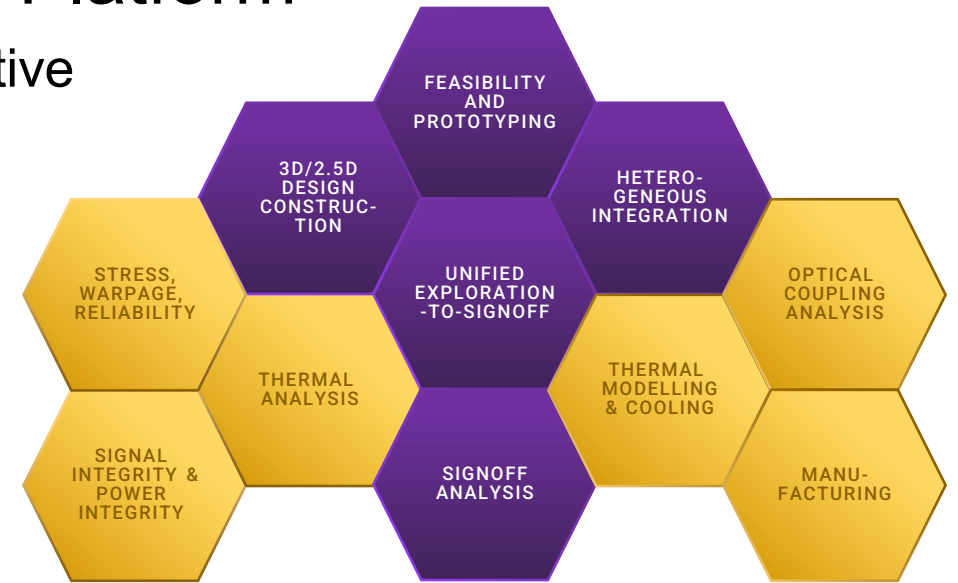


Multi-Die Not Only Integrates Chiplets,
But Also Integrates Historically
Independent Workflows

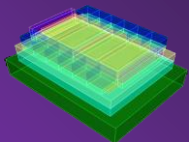
- Multi-Team
- Multi-Company
- Multi-Die
- Multi-Node
- Multi-Physics
- Multi-Objective
- System Design → Implementation → Signoff

Heterogeneous Integration Requires A New Platform

Multi-Die, Multi-Team, Multi-Node, Multi-Physics, Multi-Objective

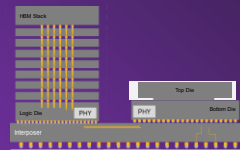


3D Stacked Design



Logic-on-Logic
Memory-on-Logic

HBM Stacks

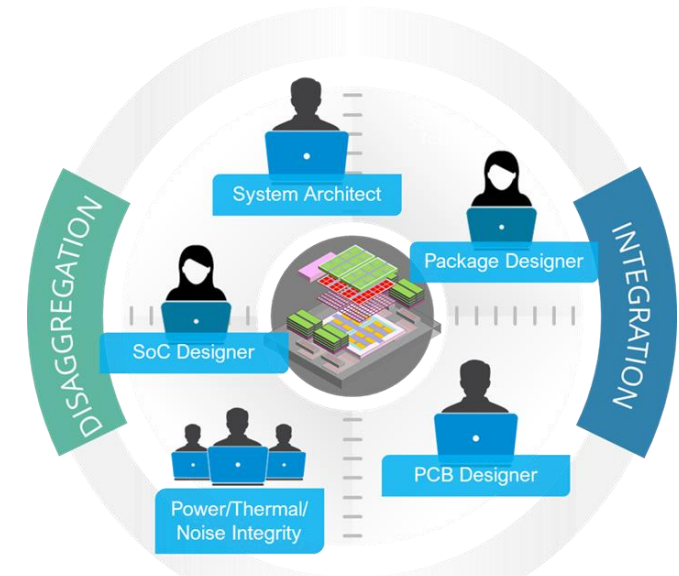


8-12 Stacks, 12-16 High
1.2 TBs/stack; 1-2 pJ/bit

Adv. Packaging

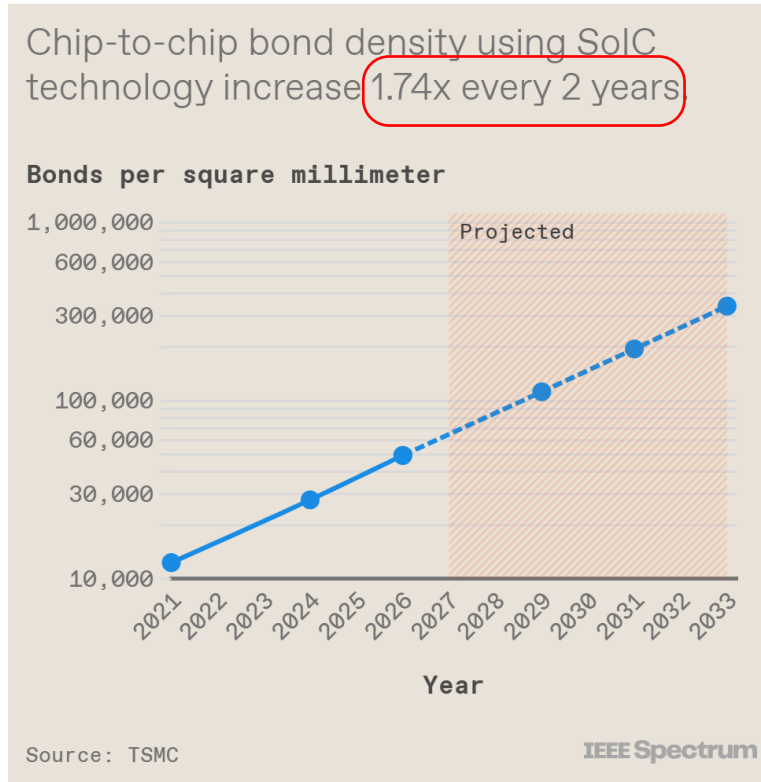


Wafer-scale Integration,
Large form-factor pkgs.



Agentic workflows aids both individual workflows and cross-domain optimization

Complexity Increasing From Relentless Scaling



Multi-Die Not Only Integrates Chiplets,
But Also Integrates Historically
Independent Workflows

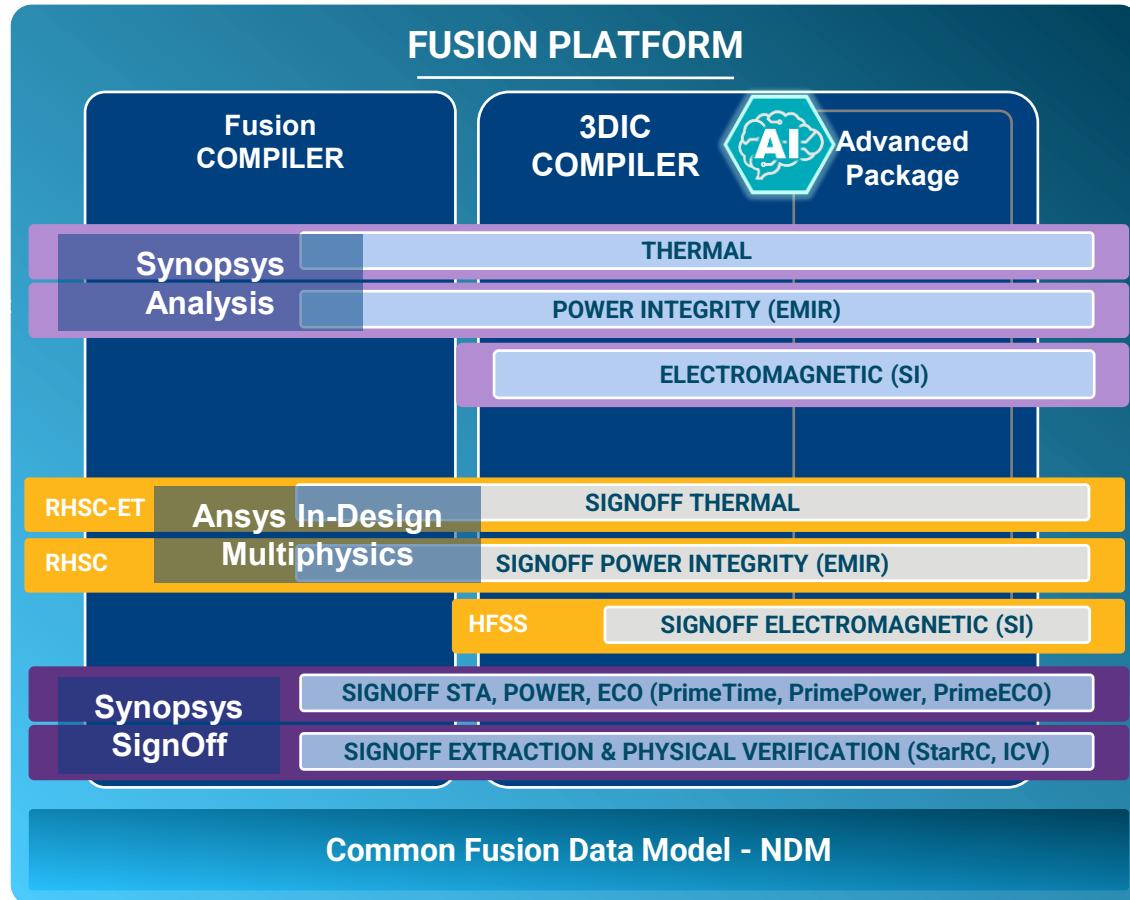
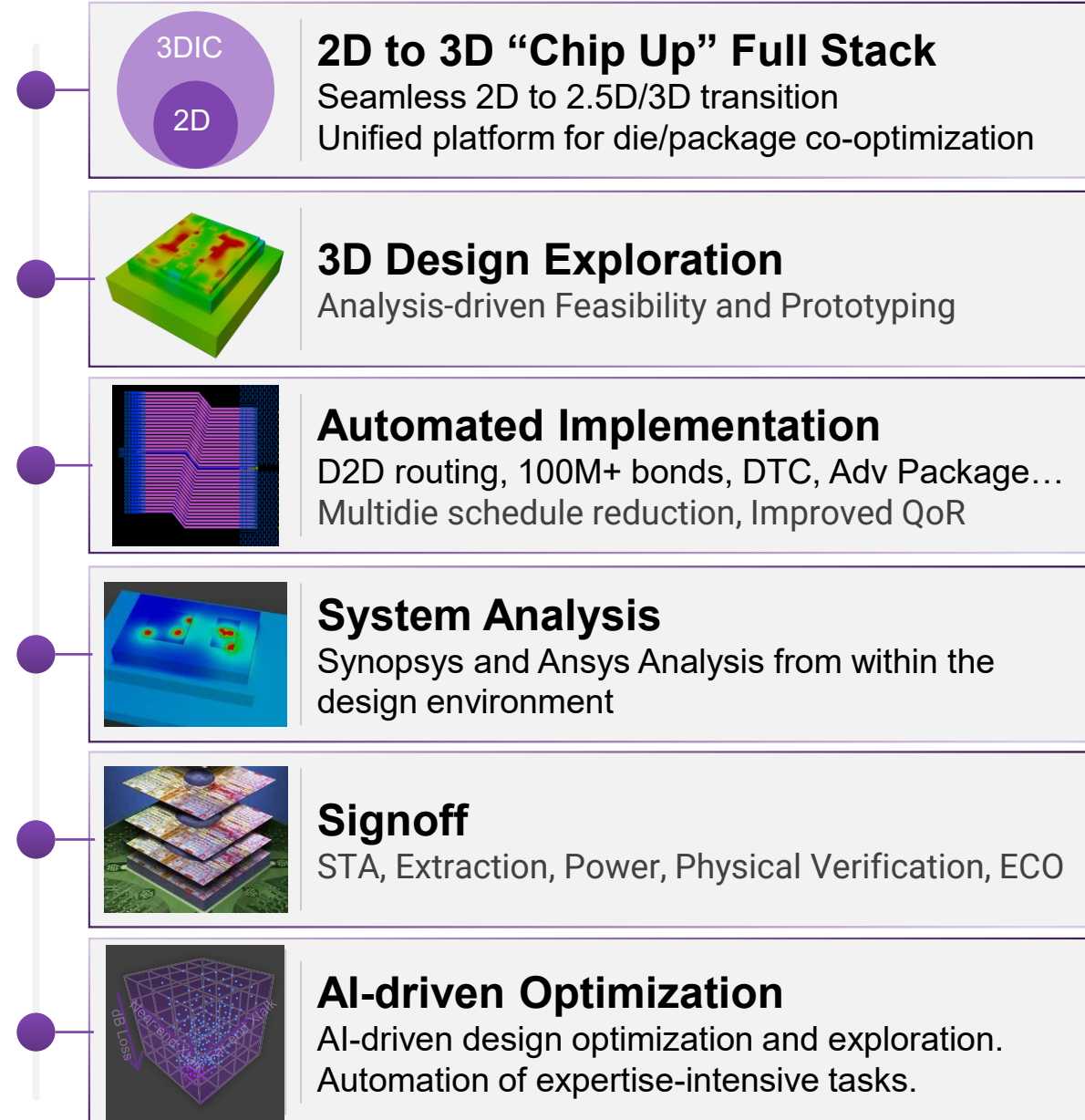
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Mark Liu, Philip Wong, How We'll Reach a 1 Trillion Transistor GPU, IEEE Spectrum

- Inter-chiplet connections primarily done manually
- Bond densities growing at exponential rate – $O(1.32^n)$
- Reticle limits continue to increase: 3.3X→5.5X→8X→50X
- Number of human fingers $O(1)$

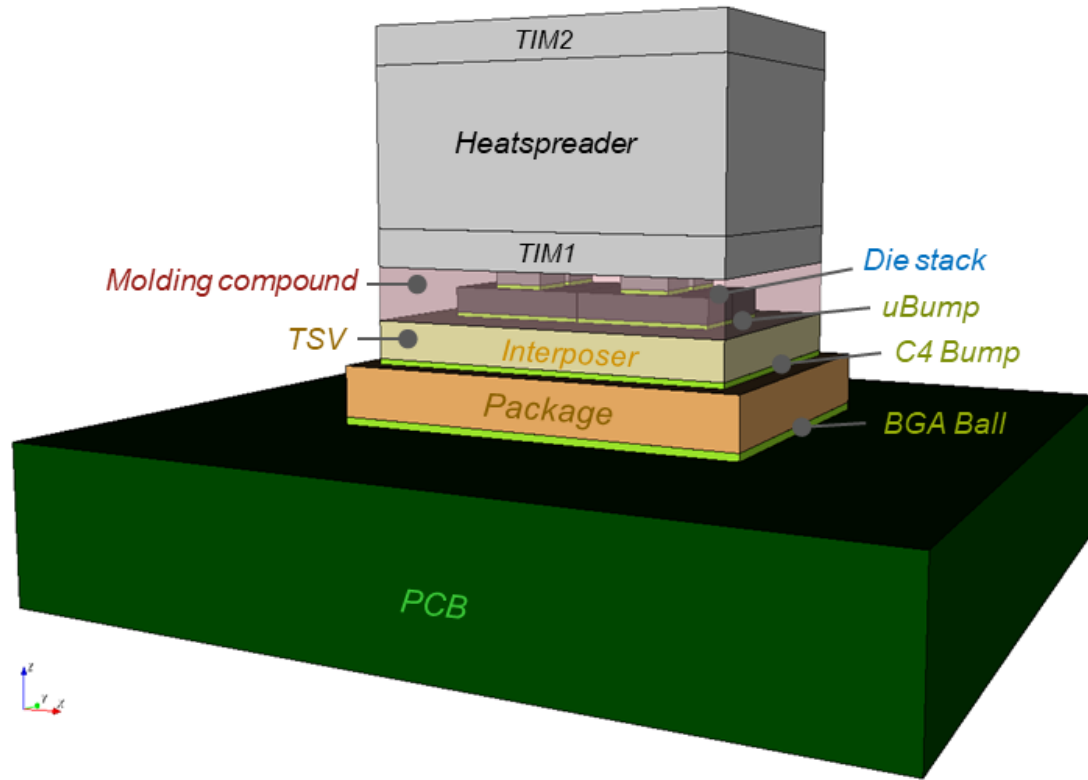
Multi-Die

Unified Platform for Analysis Driven Design and Optimization



3DIC Compiler Multi-Die Design and Analysis

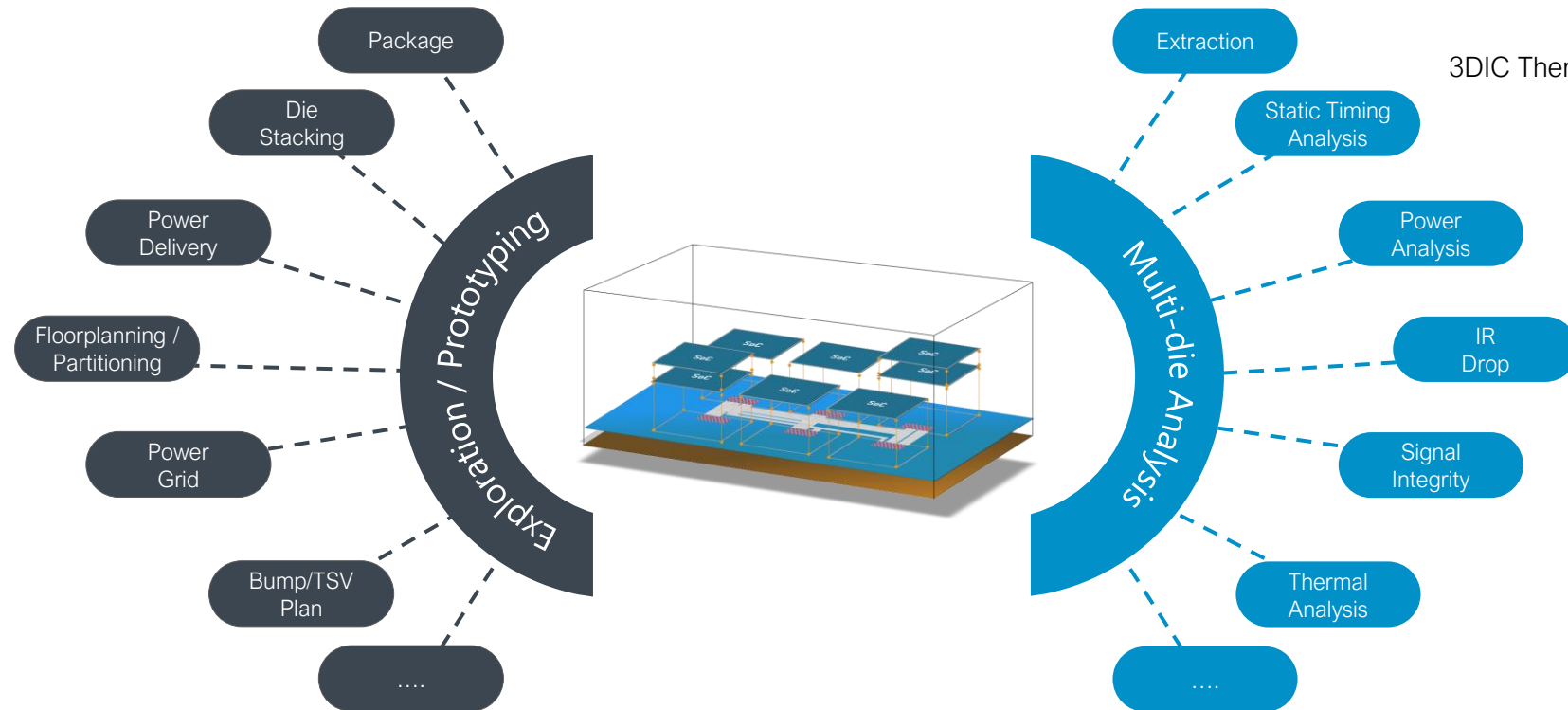
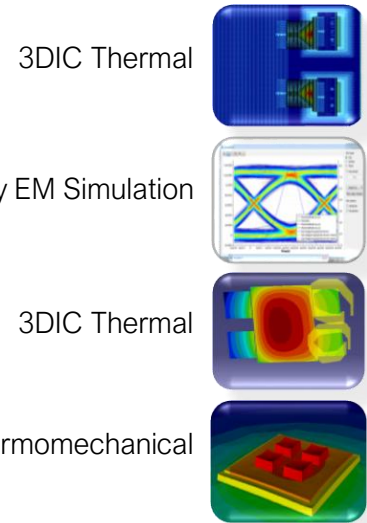
Full Stack within a Single Design/Analysis Environment



- Representation of full stack including multi-die system, thermal components, PCB, package substrate
- Die representation can be templated abstraction through fully specified die
- System Analysis within a single environment, rather than separate environment for each analysis
- Design, implementation capabilities in same single environment

3DIC System Exploration and Design

Design at the Early Stages with Minimal Inputs



EDA Advancements

Design Use Cases

Electromigration/IR Drop Prototype

- Objective
 - Understand the IR-Drop characteristics of the multi-die design

Thermal - Overview

- PDN (Power Distribution Network)
- Power Profiles/Regions
- Connectivity
 - Hybrid Bumps
 - uBumps
 - C4 Bumps
 - BGA (Ball Grid Array)
 - TSVs (Through Silicon Vias)
- Thermal Components
 - Lid (Heat sink)
 - TIM (Thermal Interface Material)
 - Substrate
 - PCB

Meta | snug

Building database

- Full testcase
 - 2 IODs, 8 SOCx, 8 HBMx, 4 dummy dies

Summary

- 3DIC will continue to grow
 - Superior scalability, computational throughput, cost balance
 - Great potential, but comes with many risks
- New IR & thermal feasibility engines in 3DIC Compiler
 - Can be used to detect inter-die conflicts
 - Our testing on real product matched well with signoff analysis
 - Quality of results will depend on quality of power data!
- Both engines are in production release and available for general use

AMD | snug

AMD | snug

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Multi-Die Partitioning and Floorplanning Prior to Netlist Using 3DIC Compiler

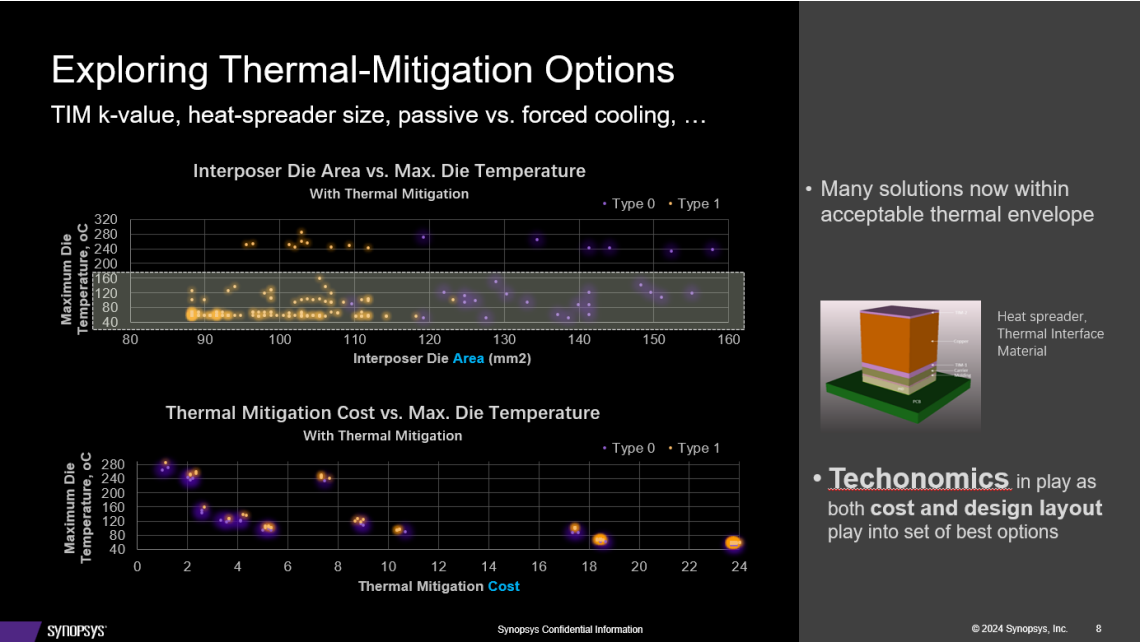
Sivanandh Ramadass
Gireesh Vijayakumar

3D Odyssey: Navigating the Depths of 3DIC Feasibility Using the 3Dblox v2.0 Framework

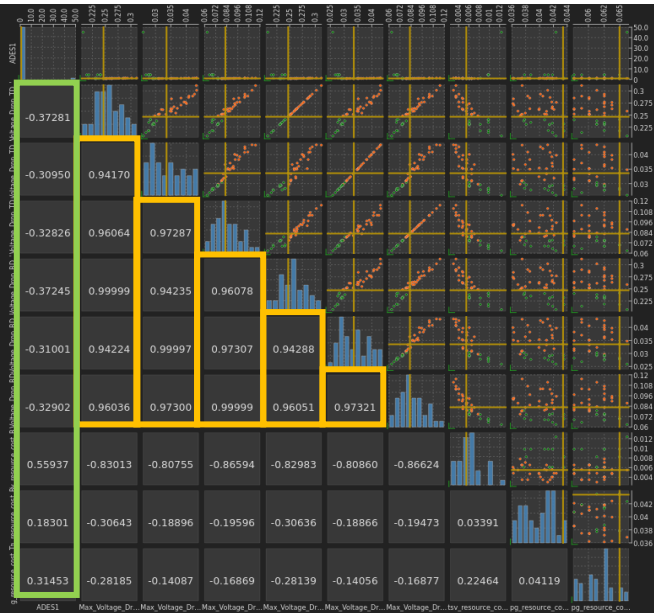
Nitin Navale
Simon Burke
Advanced Micro Devices, Inc.

EDA Advancements

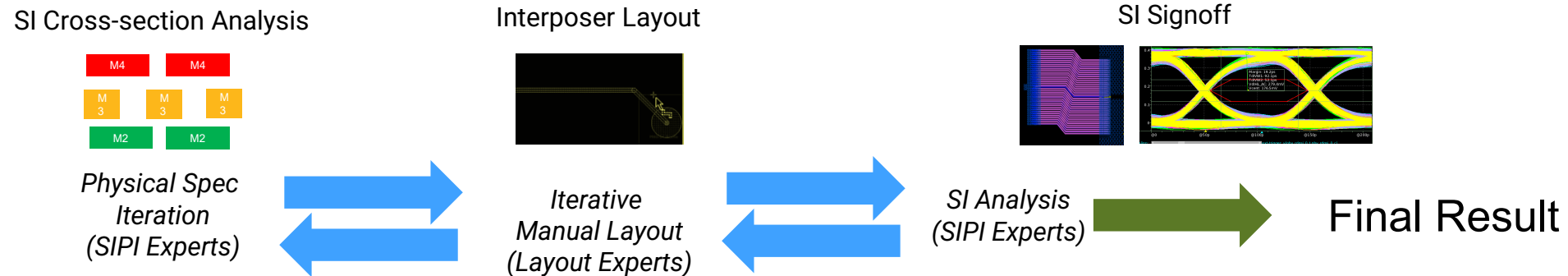
Thermal Exploration, 3DIC Compiler - A. DeGeus, IMEC Keynote 2025



ML Design Analysis and Optimization for Multiphysics - 3DIC Compiler

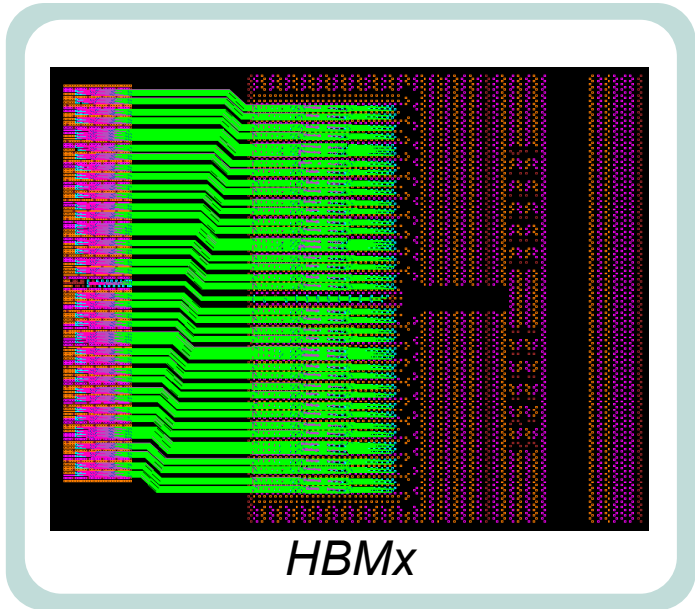


Die-to-Die Interconnect Design



- “Spec-based” Methodology, ~6 months for a full channel implementation
- Routing typically manual, 3-4 weeks for a single implementation
- Real projects usually have multiple major design changes
- Cross-section Analysis: SI-based physical spec from simulating net patterns
- Interposer Layout: Based on SI spec and rules of thumb from PCB design.
- Tedious process, increasingly difficult to converge to spec, and sub-optimal

HBMx Channel Routing



	Channel Width
HBM3/3e	1024 bits
HBM4	2048 bits

Increasing bitwidths with HBM4

- Synopsys 3DIC Compiler D2D Routing Pattern
 - Work at 7.2Gbps through SI simulation
 - Shorten channel signal routing runtime by 50%
 - Easy for channel routing balance

Source: GUC

Origin

New

HBM3 Interposer	6% width increase StatEye opening 8% average timing margin improvement
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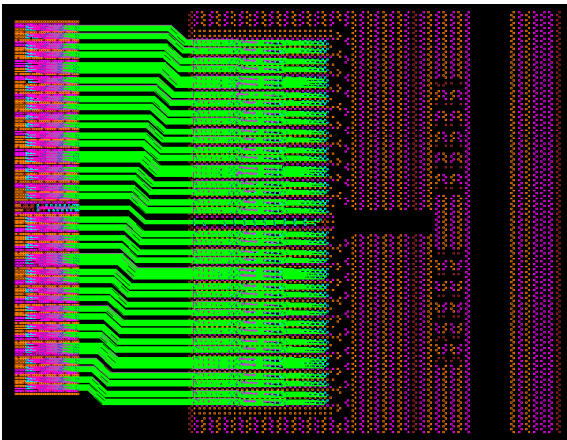
HBM3 Design	Custom Layout	Automated Routing	Compare Results
Eye Width@±60mV	59.8 ps	63.6 ps	6% better , for worst channel
Crosstalk (NEXT)	-30.9 dB	-29.6 dB	4% worse , still at good level, not hindering performance
Insertion Loss (IL)	-4.74 dB	-4.66 dB	2% better , less attenuation
Intra Channel Skew	6.5 ps	5.5 ps	15% better , less skew, worst case

Source: Synopsys

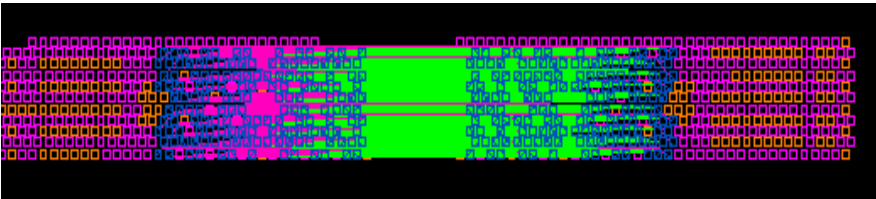
EDA Advancements

High-Speed Signal Integrity AI Optimization (ISSCC 2025)

HBMx



UCIe

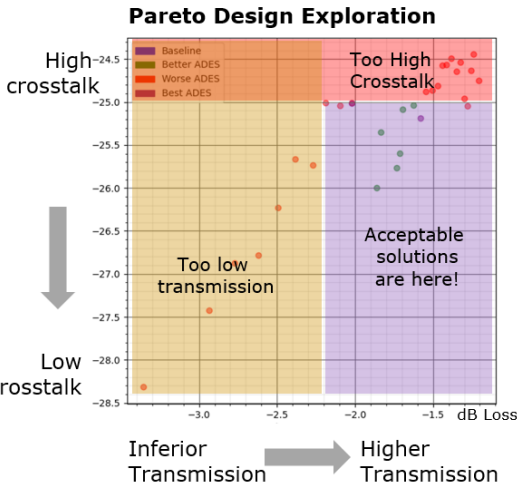


Results

Transmission Loss

	Baseline	3DSO	Improvement
Design 1 (HBM3)	-2.58 dB	-2.02 dB	0.56dB (-17%)
Design 2 (HBM3)	-2.11 dB	-1.88 dB	0.23dB (-8.7%)
Design 3 (UCIe)	-0.82 dB	-0.81 dB	0.01dB (-1.1%)
Design 4 (HBM3)	-1.27 dB*	-1.21 dB	0.06dB (-4.1%)
Design 5 (UCIe)	-0.88 dB**	-0.77 dB	0.11dB (-11.4%)

*3DICC baseline is better than original custom db (6% eye width, 8% timing)
**3DICC baseline is better than original custom db (2% IL, 17% jitter)



Unified Engineering Knowledge

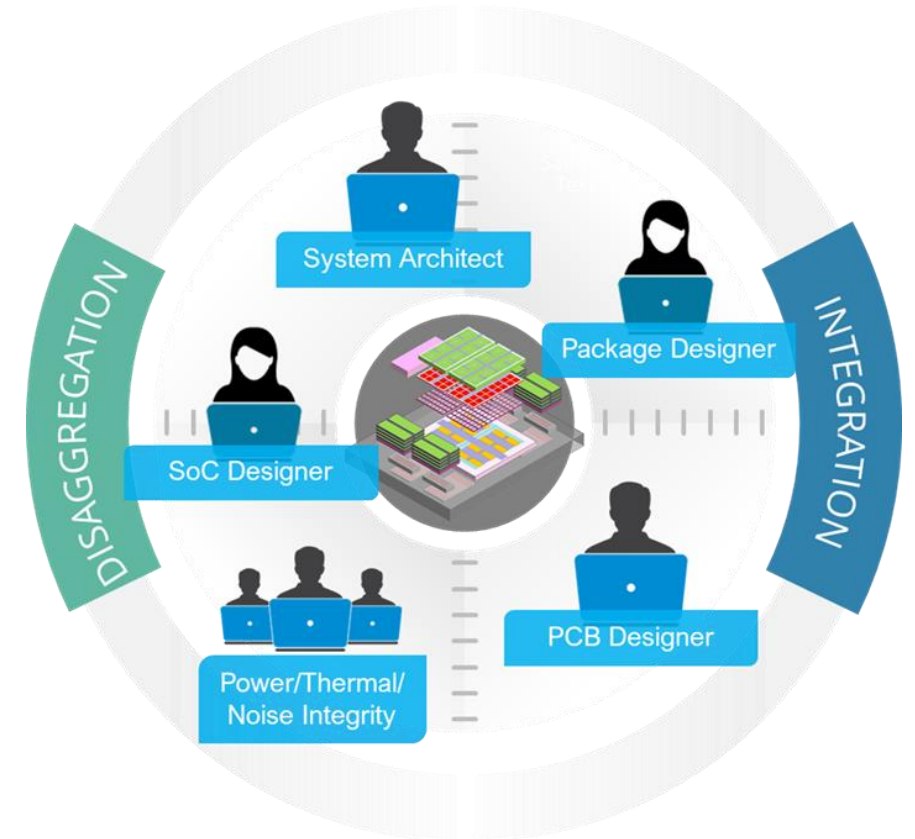
Unified Platform Still Requires Unified Knowledge

A unified platform integrates the engineering capabilities but doesn't integrate engineering knowledge.

This is very real.

- Working across silo'ed functions requires engineering knowledge
- Workflows can stay fragmented even if tooling is unified
- Many handoffs, workflow hits non-technical bottlenecks
- Sub-optimal results, not fully leveraging unified platform
- High technical and schedule risks, and these are increasing

Problem → platform → automation → expertise bottleneck → AI



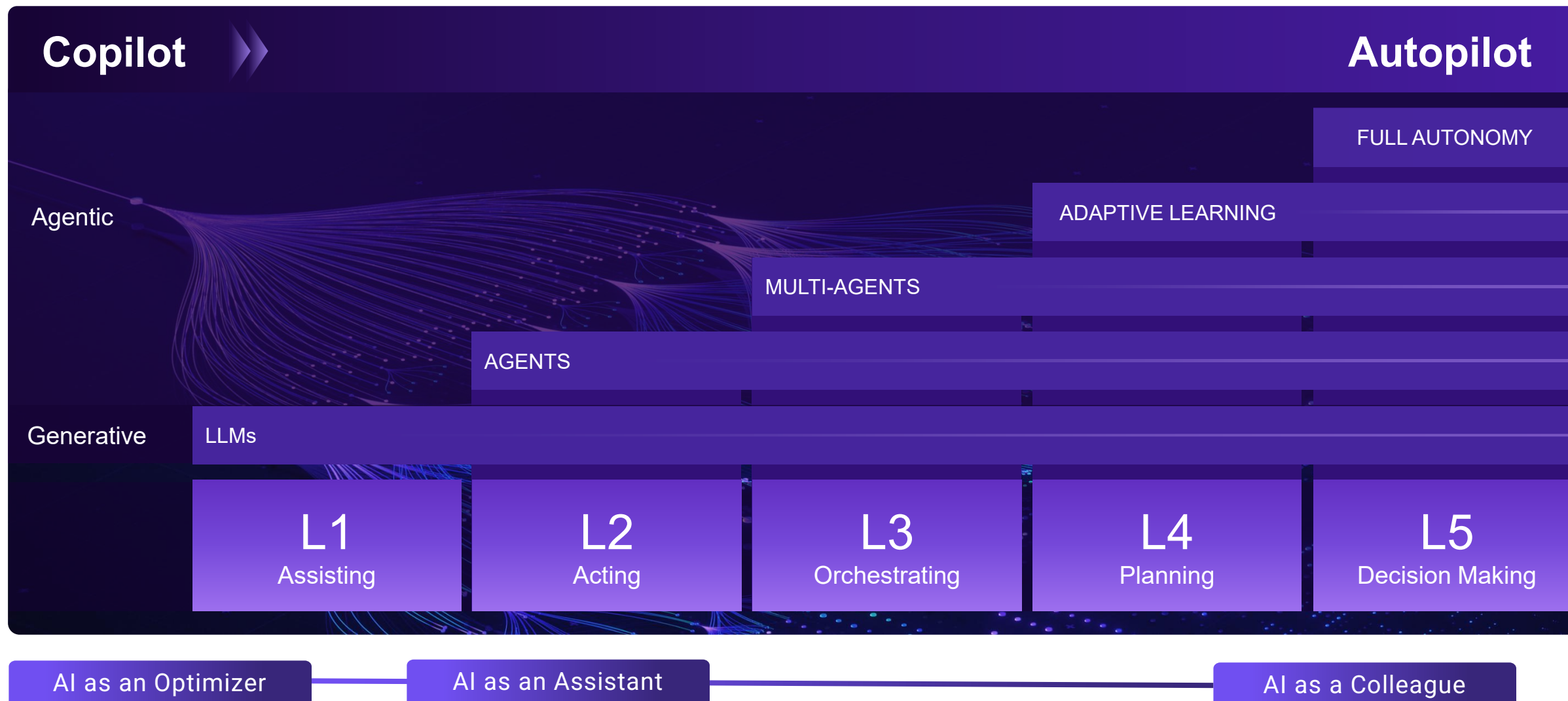
Industry Workflow Transitioning Happening

EDA, Design and Manufacturing Inextricably Linked

Complex industry transitions happening:

- Fully Manual → Automation
 - Many Single Domain Problems → Cross-Domain Problems
 - Experience Driven → Analysis Driven
 - Assembly → Automation and System Optimization
 - AI Assisted Cross-Domain Exploration
 - Organizational Alignment
-
- How does the industry jointly make these transitions
 - Incremental improvements: Are happening. However, complexity is scaling faster than workflow productivity.
 - Transformational improvements: Efficiency and Optimality requires new tooling, new methods, automation, system optimization, cross-domain workflows, AI-frameworks including Agentic. Many of the industry's leading design teams are partnering across EDA, design and manufacturing to define this together with overall semiconductor readiness.

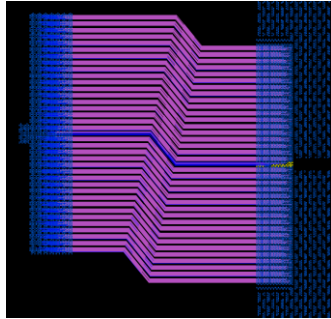
The Progression from Assistive to Agentic AI



High Performance D2D Multi-Agent Workflow

Three Compartmentalized Disciplines in One Workflow

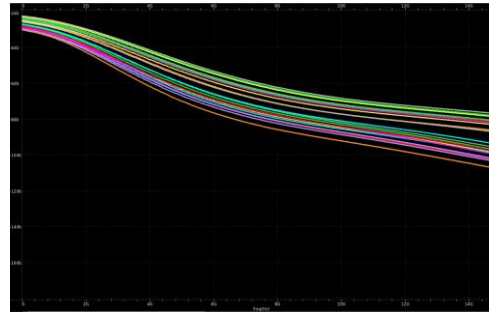
*Physical Implementation
(Layout)*



HBM/UCle Routing
Layout

Route
Agent

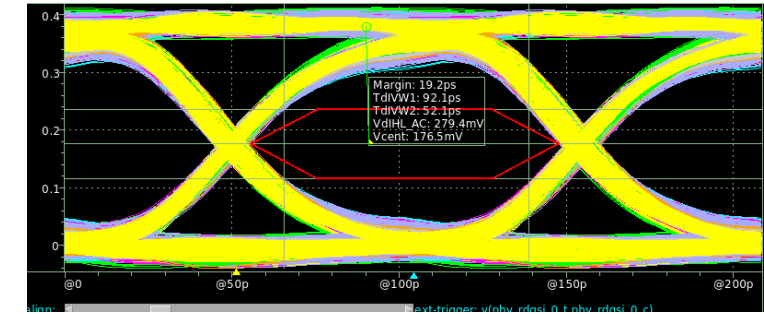
*High-Speed Extraction
(Frequency Domain)*



HFSS Extraction
S-parameters

Extraction
Agent

*Simulation
(Time Domain)*



PrimeSim, Waveview
Eye Measurement

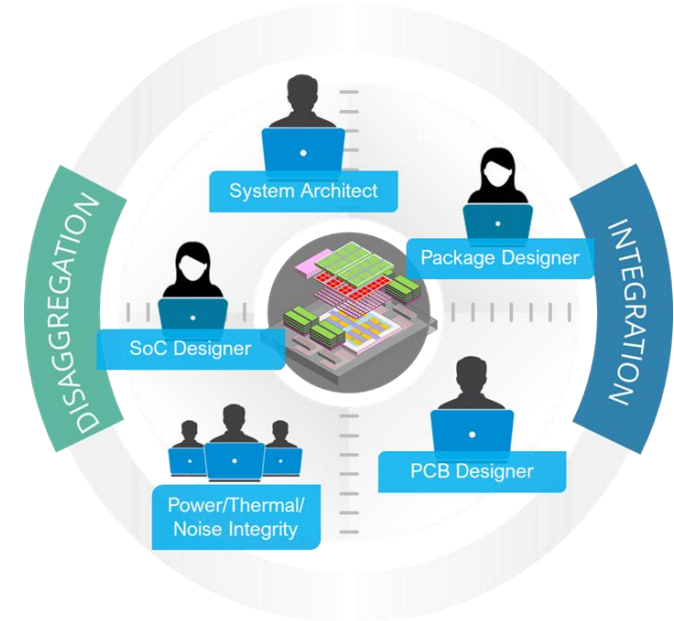
Simulation
Agent

- **Cross-Domain:** Enables domain experts to access cross-domain workflows
- **Tedious:** Large data sets, error-prone
- **Manual Intensive:** Design Flow dominated by human time vs machine runtimes

Lessons Learned

Technology Partnerships with Customer 3DHI Design Teams

- AI needs rigor on what is “good”
 - Formalization of methods – Single Source of Truth
 - Deterministic, Codified Objectives
 - These are practices that “should” already be in place
- Methodology change is a transformation
 - These are not the usual incremental improvements
 - Mindset shift
 - Agentic and Natural Language democratizes technology
- EDA and Agentic AI will transform the way we do analysis and design. Scaling demands it.
 - Not “IF” but “WHEN”



Agentic workflows aids both individual workflows as well as cross-domain optimization

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