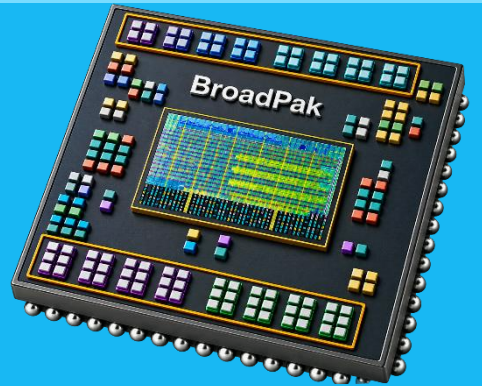
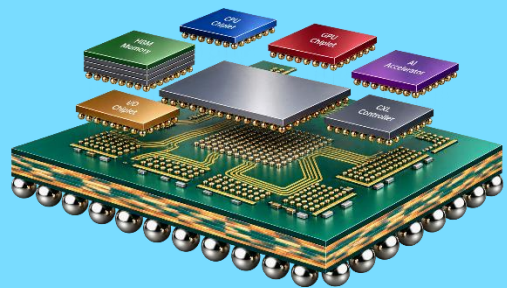




ADVANCED SUBSTRATES: THE FOUNDATION FOR SCALE-IN, SCALE-UP, SCALE-OUT, AND OPTICAL AI INFRASTRUCTURE



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OUTLINE



01

AI Scaling & Memory Wall

Model growth, context windows, KV cache, and infrastructure pressure

02

Advanced Substrates as AI/memory Fabric

Scale-in, scale-up, scale-out and optical-ready platforms

03

Wafer-Level & Si-Core Substrates

Density, body size, routing, wide/slow vs. narrow/fast options

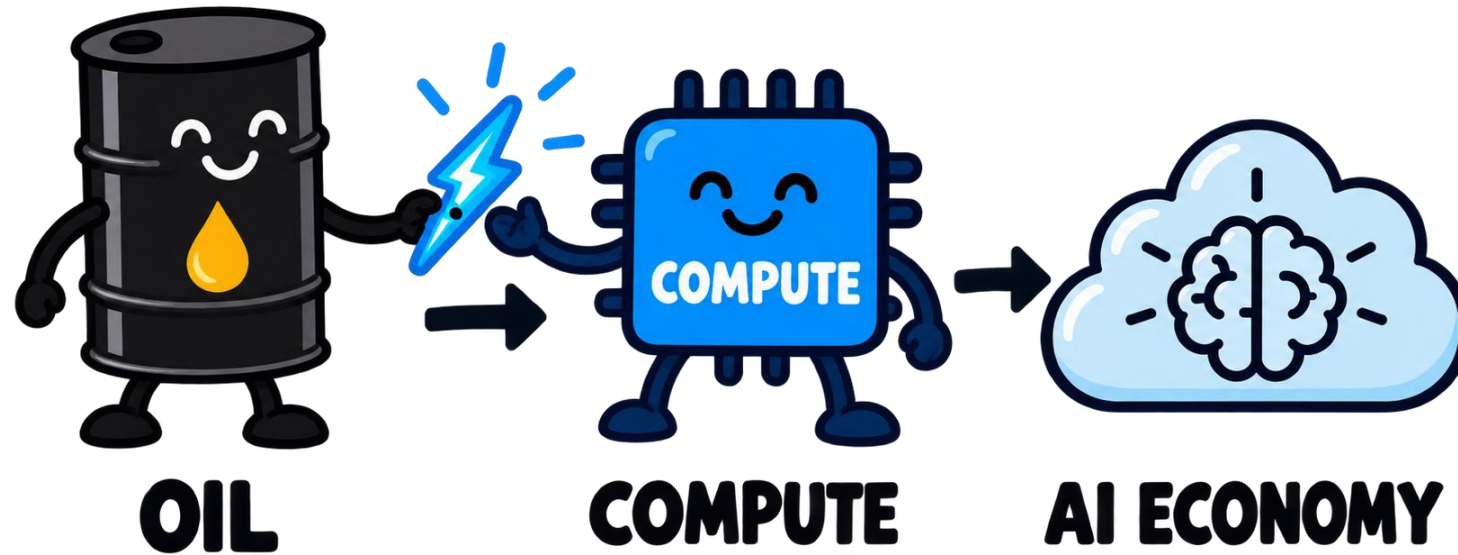
04

Fan-Out, CPO & Roadmap

WLP/PLP, 3D PLP, and photonic package integration path

AI AND OIL: A SYMBIOTIC

COMPUTE IS THE NEW OIL

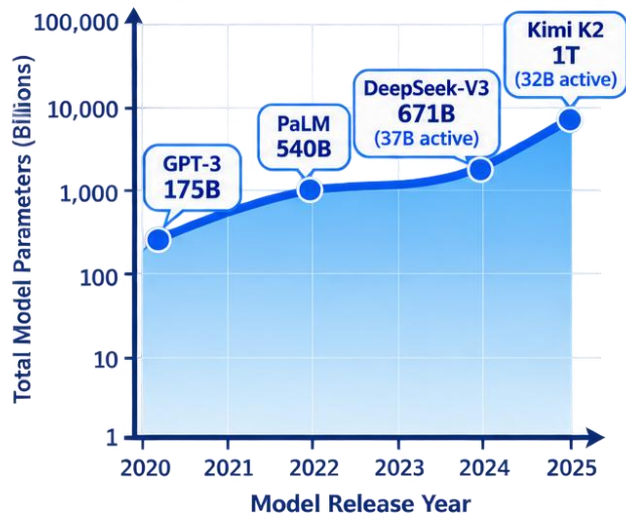


AI SCALING: KV Cache Pressure

Model Scale ↑ → **Context Length** ↑↑ → **KV-Cache Pressure** ↑↑↑

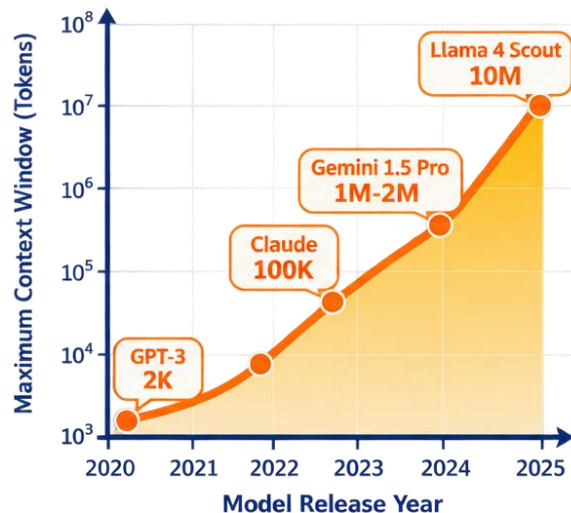
1. Model Parameter Growth

Frontier model parameter counts (publicly disclosed)



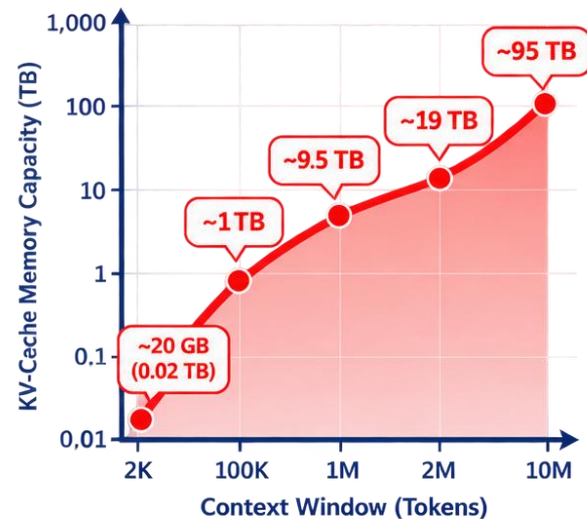
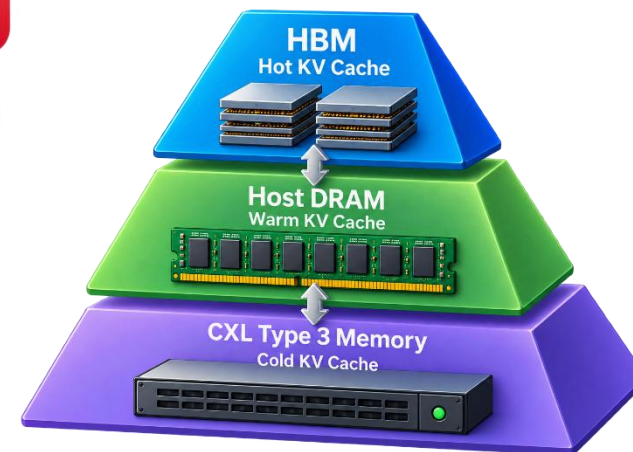
2. Context-Window Growth

Frontier model maximum context length (publicly disclosed)



3. KV-Cache Capacity Pressure

Illustrative KV-cache capacity at 32 concurrent sequences

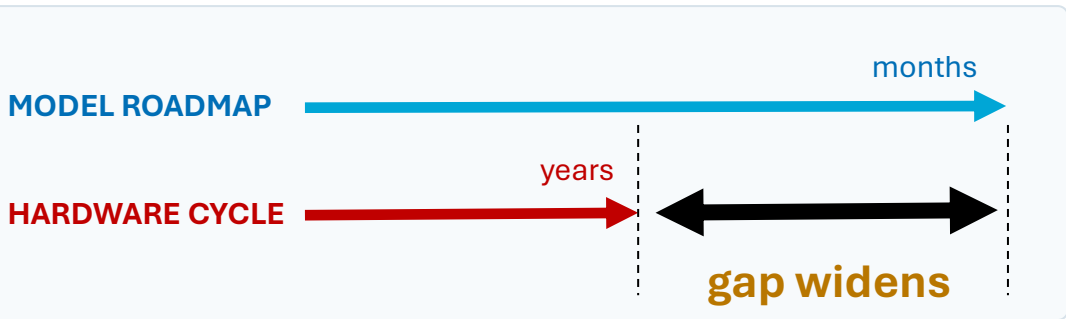


Models Evolve Faster Than Hardware

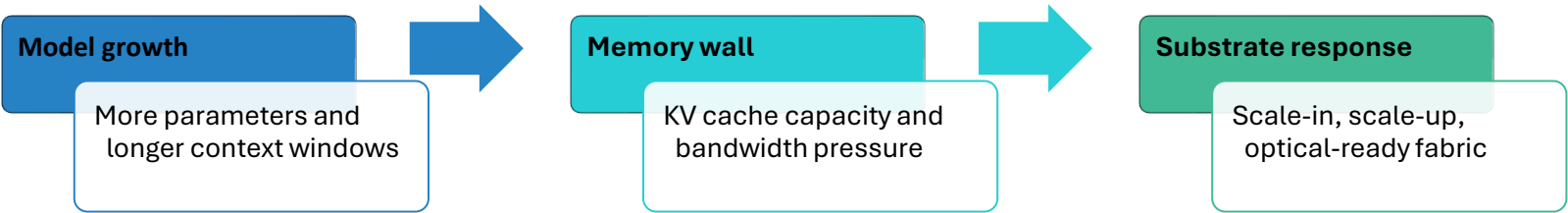
AI model roadmaps move at software speed;
Packaging, memory, and substrates must close the hardware gap.

Fact

The substrate is becoming the AI infrastructure layer that absorbs bandwidth, power, thermal, and memory-growth pressure.

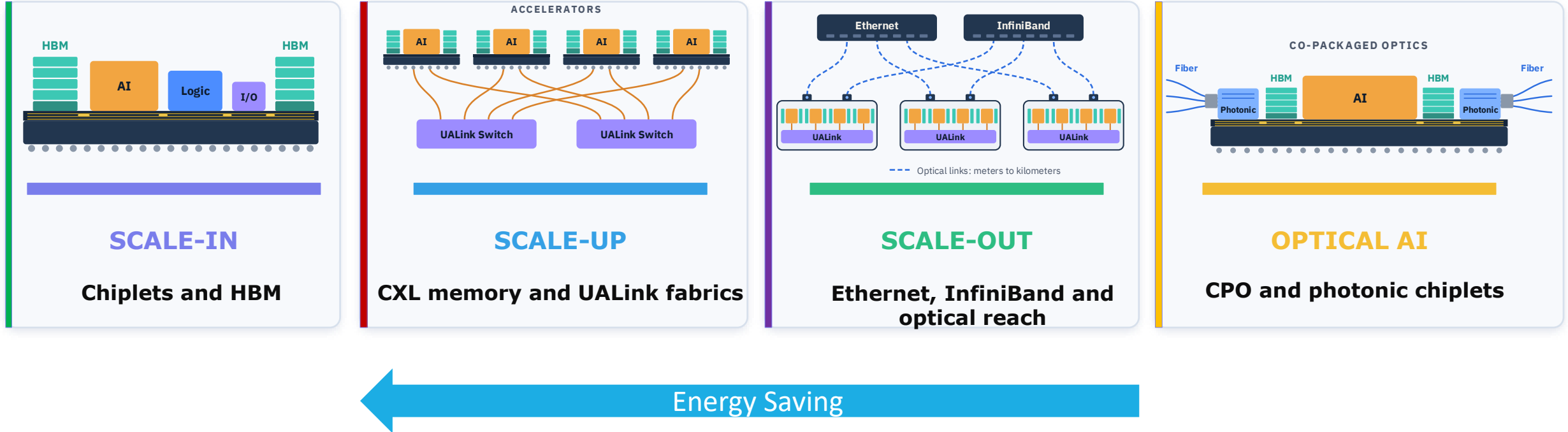


Advanced substrates and packaging bridge the widening memory wall.



ADVANCED SUBSTRATES ARE THE FOUNDATION FOR AI SCALING

The substrate defines what the AI system can become

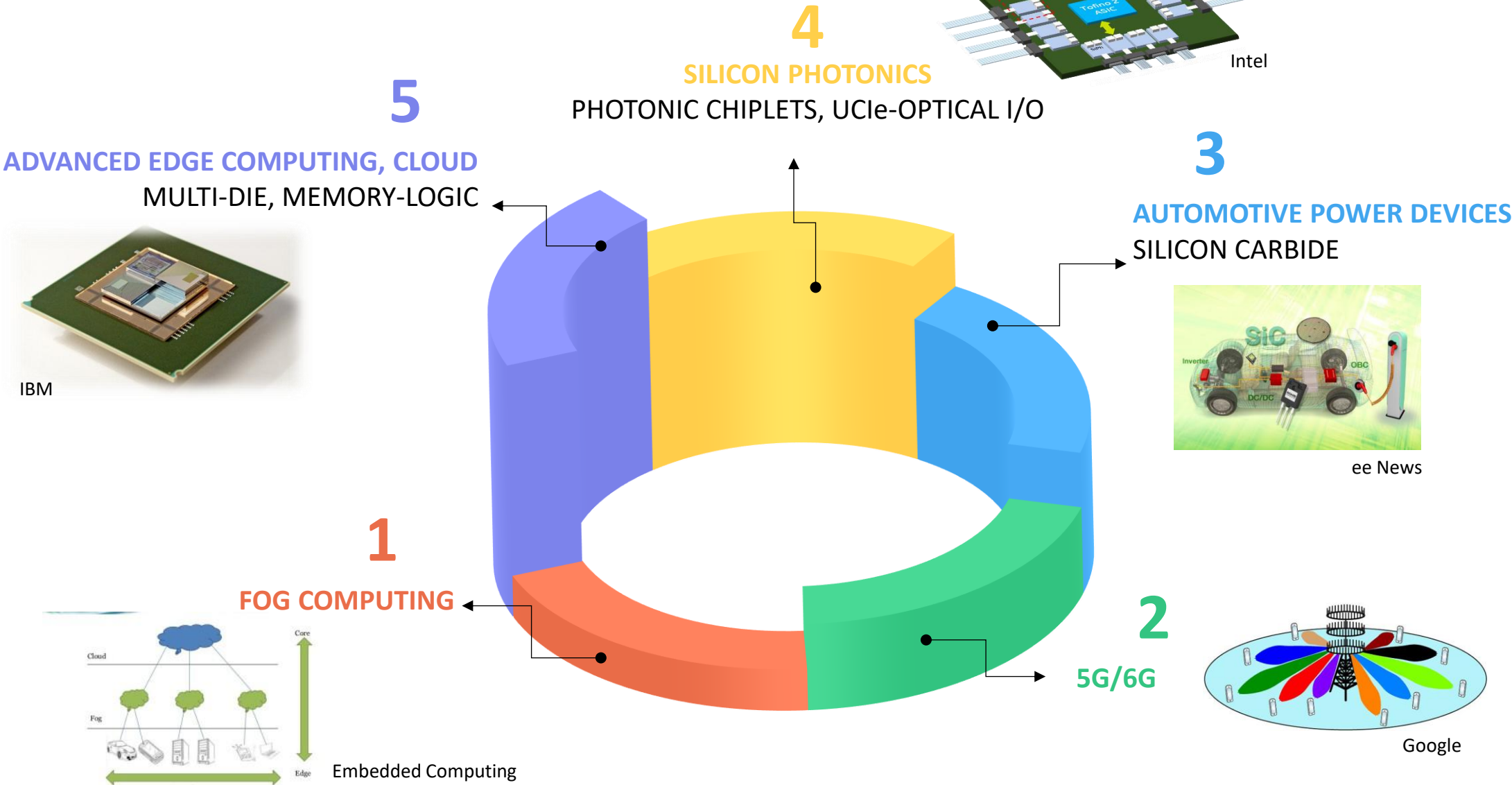


AI SCALING

Substrate architecture, multi-physics design and manufacturing strategy must be developed as one system.

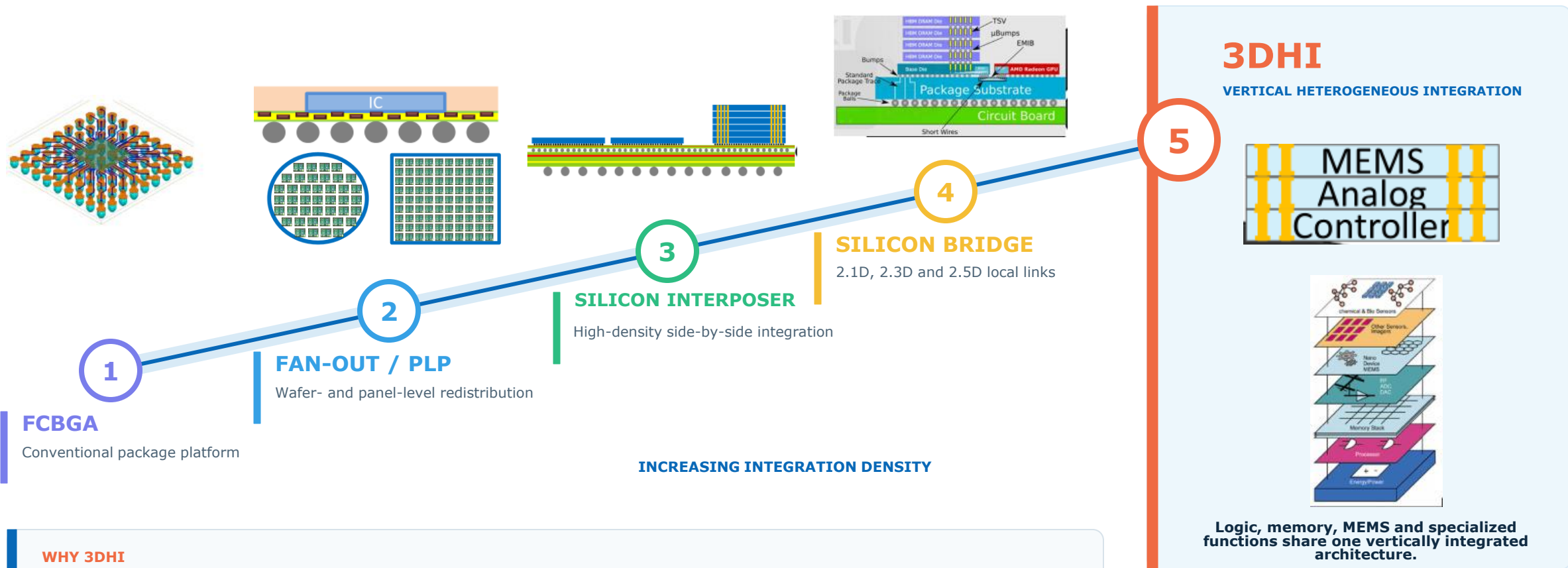
CHANGE IN MEGATREND PATTERN

BASED ON A CORPORATE DESIGN LOAD PERSPECTIVE



Packaging integration is moving from side-by-side placement to 3DHI

BroadPak supports the design continuum from conventional packages to vertically integrated heterogeneous systems.



WHY 3DHI

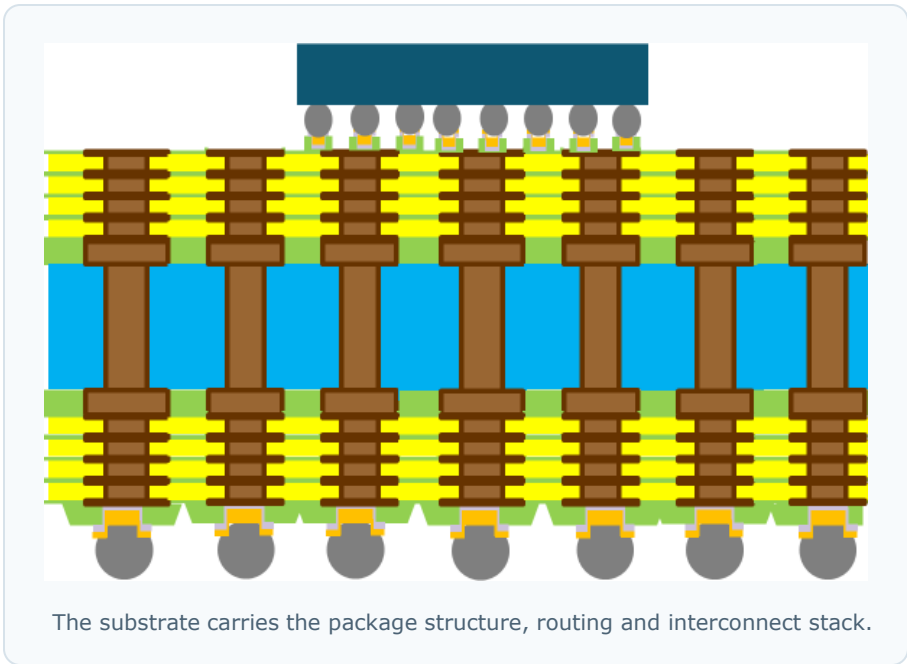
3DHI adds the vertical dimension to extend integration density beyond side-by-side architectures.

BroadPak integrates package architecture, interconnect, power, thermal design and manufacturing constraints.

Substrate materials define the package-size ceiling

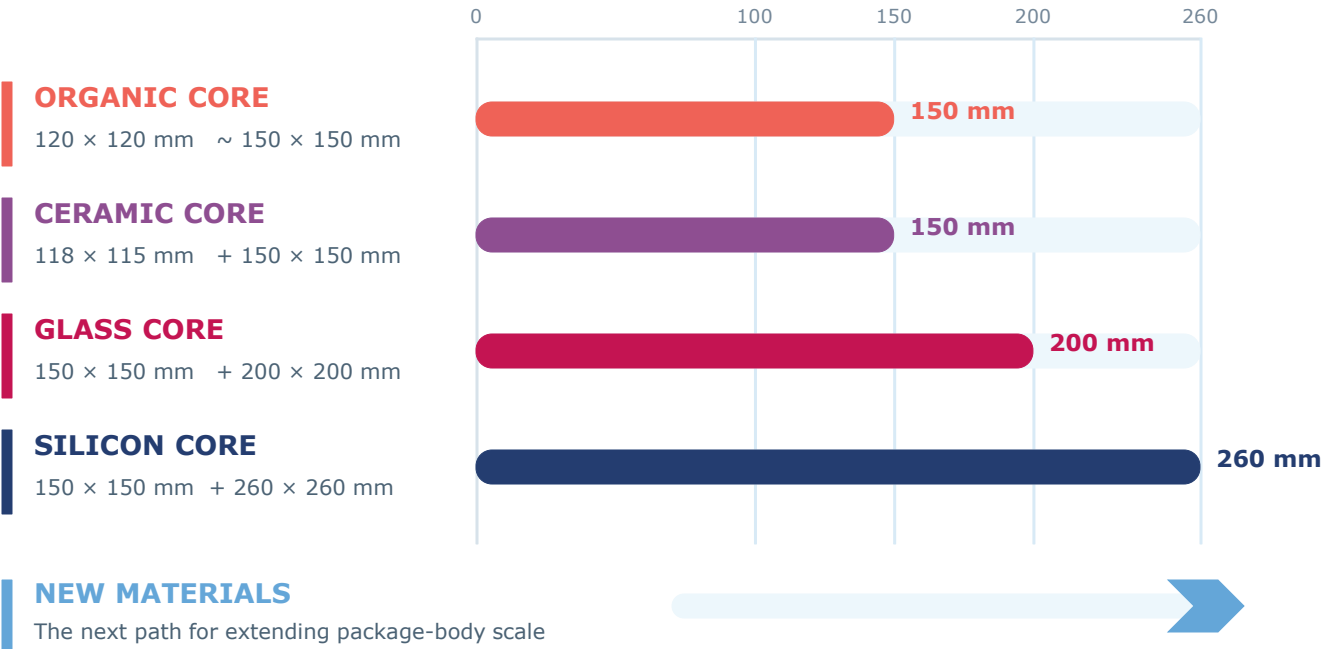
As package bodies grow, core material selection becomes a primary design constraint.

PACKAGE SUBSTRATE CROSS-SECTION



REPRESENTATIVE PACKAGE BODY SIZES

Bar length represents the larger listed edge, in millimeters



DESIGN IMPLICATION

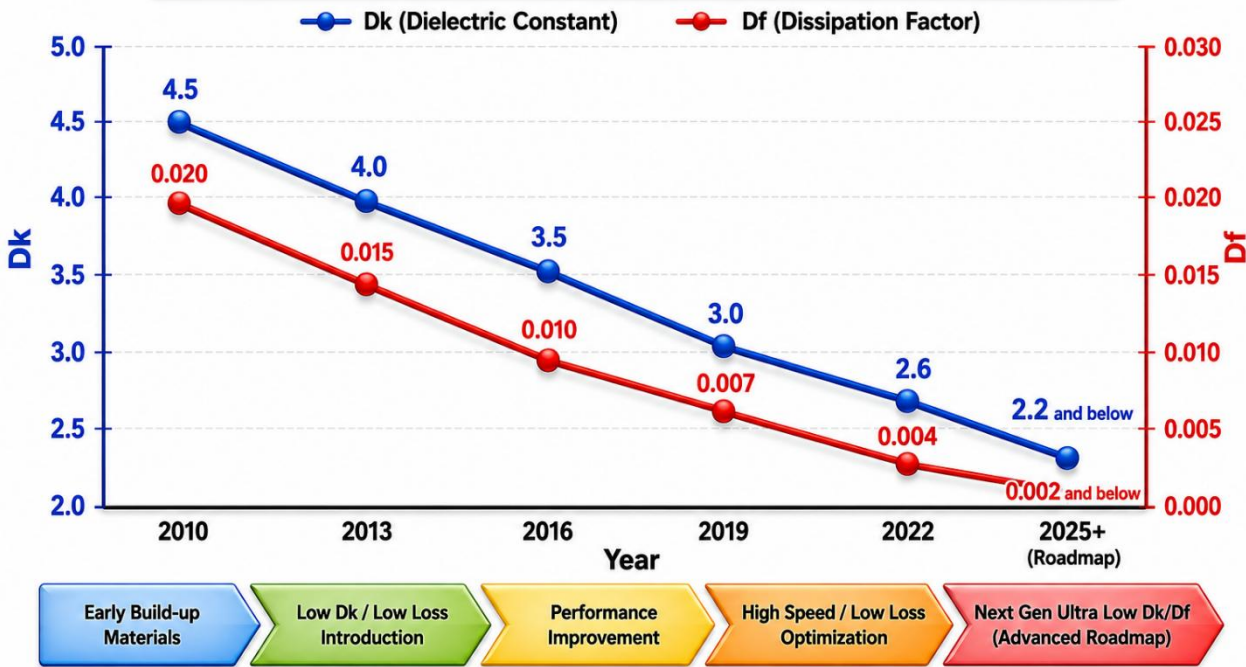
The package substrate becomes a primary scaling constraint as body size grows.

Core material sets the dimensional envelope for high-density heterogeneous integration.

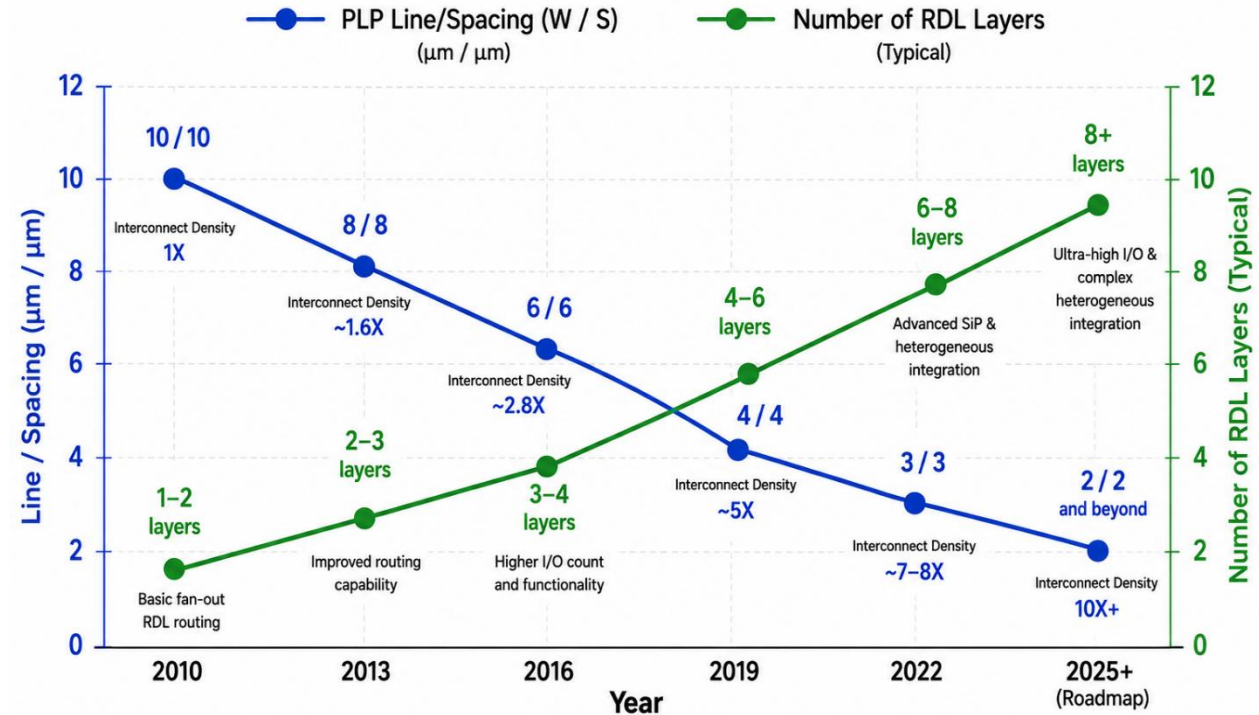
WHAT ARE DESIGNERS LOOKING FOR?

Build-up Material Dk and Df Trend Over the Years and Roadmap

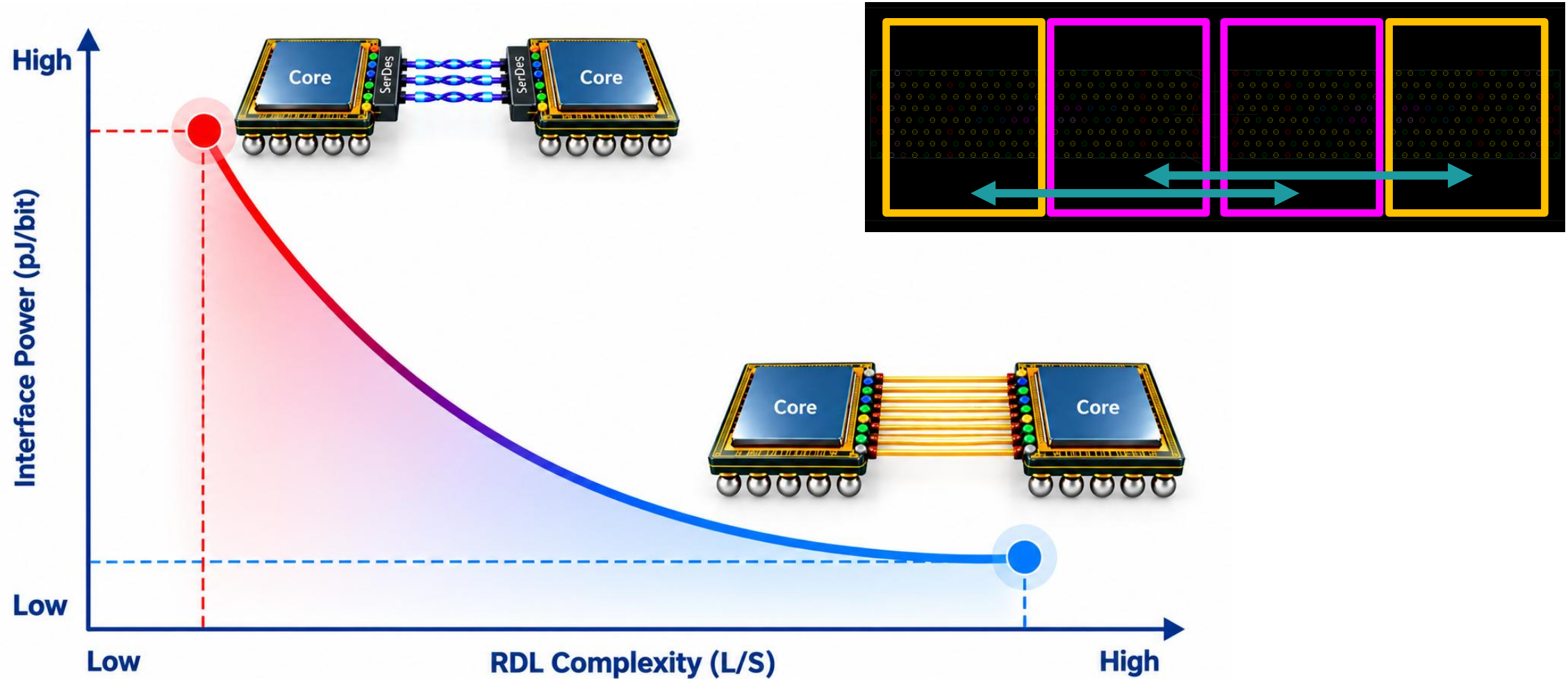
Lower Dk and Df enable higher speed, lower loss and better signal integrity



PLP Line/Spacing and Number of Layers Evolution and Roadmap



Substrate Complexity: Wide and Slow V.S Narrow and Fast



The Substrate Landscape at a Glance

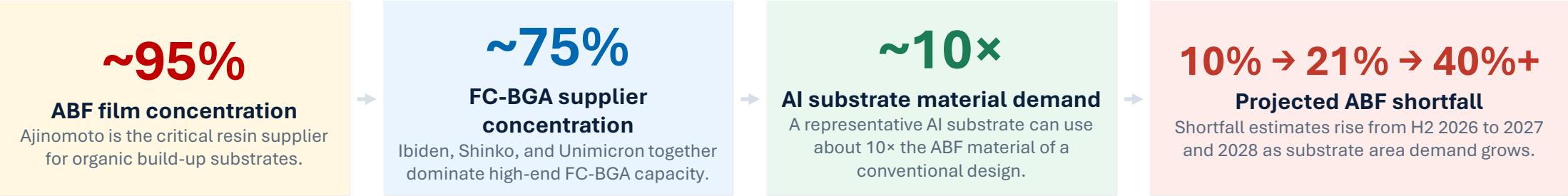
Type	CTE match to Si	Max practical size	Interconnect density	HVM status
Organic (ABF / FC-BGA)	Poor (Cu ≈ 17 ppm/°C)	~100–130 mm / side (roadmap)	8/8 μm line/space (→6/7μm)	In production — today's dominant substrate
Silicon interposer (2.5D)	Excellent (~2.6 ppm/°C)	Reticle-limited; stitched to multi-reticle	Sub-2 μm RDL, near on-die density	In production — high-end AI GPUs, costly
RDL interposer / bridge	Good (no full-Si cost)	Local, bridge-scale routing	High, but narrower than full interposer	In production — cost-optimized alternative
Glass core	Excellent (~3 ppm/°C)	Panels to 510×515mm+ (→600×600)	Up to ~10× organic (fine RDL + TGV)	Pilot through 2026; HVM 2027–28
Silicon-core / wafer-level	Excellent	Emerging — largest long-term potential	Highest long-term potential	Early-stage / R&D

“HVM” = high-volume manufacturing. Organic remains the volume workhorse; glass and silicon-core are the two leading contenders to succeed it at the high end.

The Substrate Supply Chain — and Its Crunch

Supply chain pressure points

Key message: substrate capacity is becoming AI infrastructure capacity.



A single point of concentration: Ajinomoto

Ajinomoto controls roughly 95% of the ABF film market — the resin that every organic substrate maker laminates onto its core. It raised film prices ~30% in Q3 2026 alone.



ABF substrate makers

Ibiden, Shinko, and Unimicron together hold roughly 75% of the FC-BGA substrate market; AT&S and Nan Ya PCB are scaling aggressively to add capacity.



Glass & silicon ecosystems

Corning, AGC, SCHOTT, NEG (raw glass); Absolics/SKC, Samsung, LG Innotek, Intel, TSMC (glass substrates/interposers); TSMC, Intel, Samsung (silicon interposers & hybrid bonding).



The widening shortfall

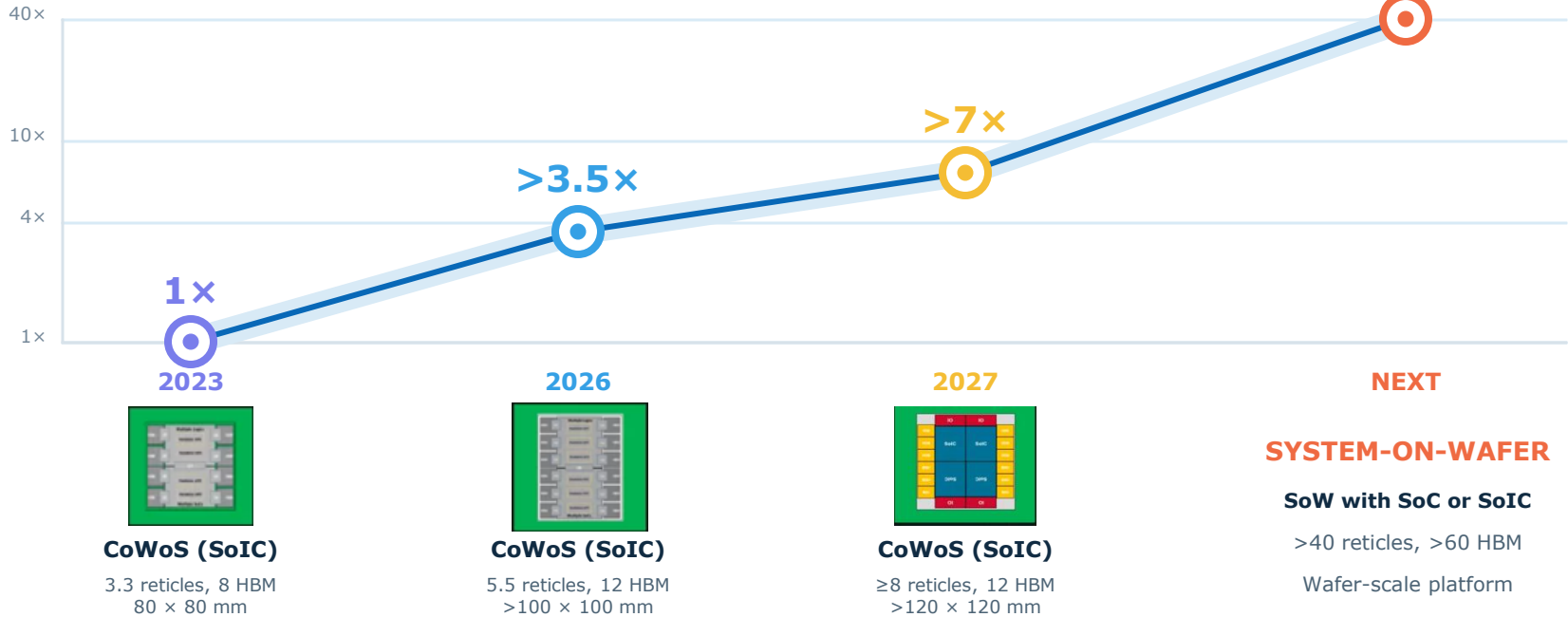
Projected ABF shortfall: ~10% (H2 2026) → ~21% (2027) → 40%+ (2028), as substrate area demand grows ~39% CAGR; A representative AI substrate now uses ~10× the ABF material of a conventional design.

TSMC is moving advanced packaging toward wafer-scale systems

CoWoS increases package scale through 2027. System-on-Wafer targets the next step in compute integration.

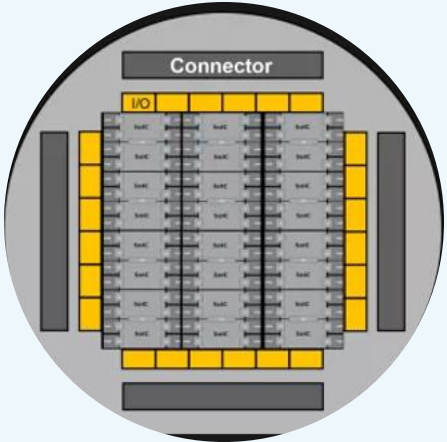
RELATIVE COMPUTE POWER

Log scale, 2023 CoWoS baseline equals 1×



SYSTEM-ON-WAFER

Package scale expands to the wafer



TARGET DIRECTION

More than 40 reticles and more than 60 HBM stacks on one integrated platform.

DIRECTION OF TRAVEL

Advanced packaging scale is shifting from larger substrates to wafer-scale integration.

The roadmap raises compute power by increasing reticle count and the number of integrated HBM stacks.

Emerging Substate Innovation: Wafer-Level-Substrate (WLS)

Bandwidth and chiplet scale are driving substrate transformation

Memory/logic links (memory wall), photonic CMOS integration and 2D/3D chiplets are pushing packages toward near-monolithic integration.

QUALITATIVE DIRECTION

Increasing integration density and system scale

MARKET PULL

Memory to logic
bandwidth

Photonic CMOS
integration

2D/3D die-to-die
chiplets



WHAT THE SUBSTRATE MUST DELIVER

Requirements intensify together as integration advances

INTERCONNECT DENSITY

- Sub-1/1 μm line and space
- Padless vias sized to line width
- Fine bump pitch support

SCALE AND RELIABILITY

- CTE matched to the device
- Rigid support for large package bodies
- Modular test access

PERFORMANCE AND COST

- Thermal conductivity and RF performance
- Cost-competitive implementation

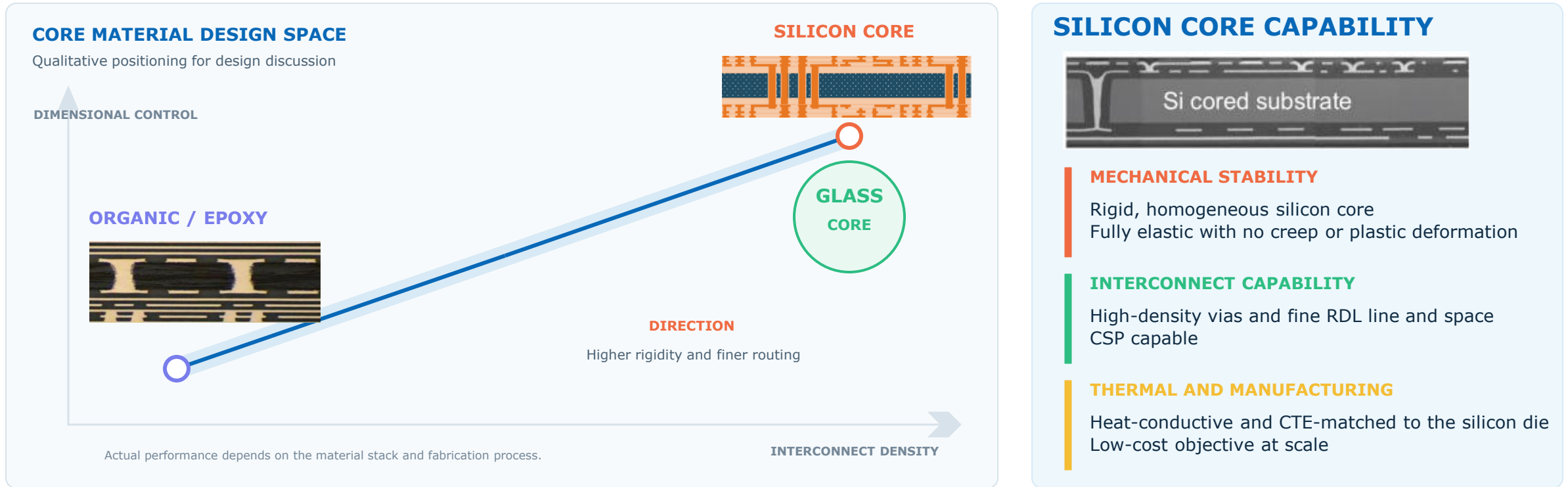
DESIGN DIRECTION

The substrate is becoming the integration platform for near-monolithic systems.

Routing density, body size, thermal behavior and electrical performance must advance together.

Wafer-level substrates are expanding beyond organic cores

Rigid glass and silicon cores extend dimensional control for larger bodies and finer interconnects.



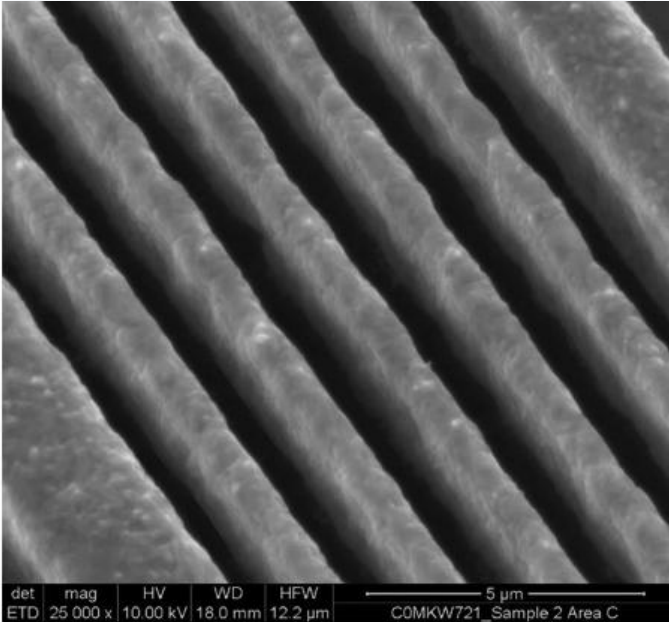
MATERIAL DIRECTION

Core material selection now sets the wafer-level substrate design envelope.

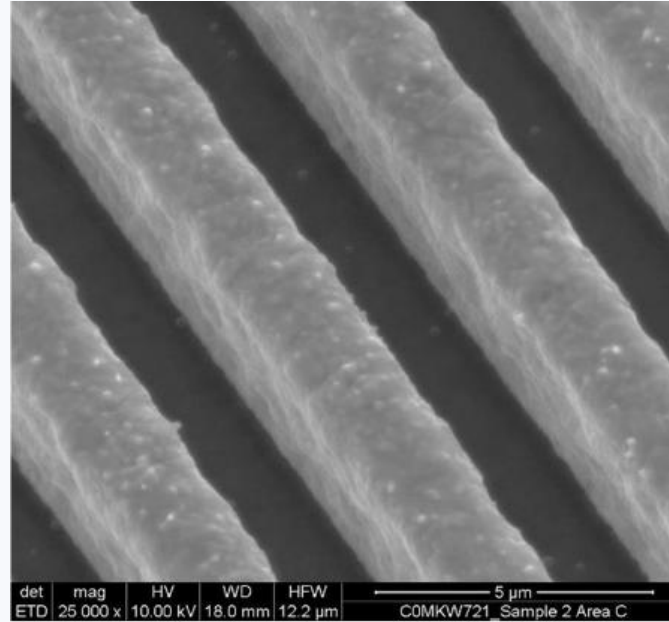
The choice links rigidity, CTE, routing density, thermal behavior and manufacturing cost.

Fine L/S with Dual-Sided Semi-Additive Flow on Wafer-Level Substrates

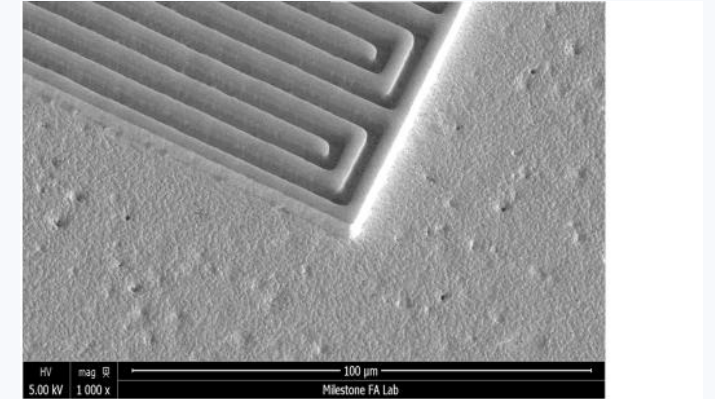
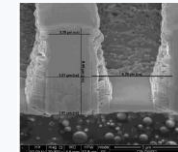
After etching
0.9 μm L/S



After etching
2 μm L/S



After etching
3 μm L/S



Trench sidewall profile (cross-section)

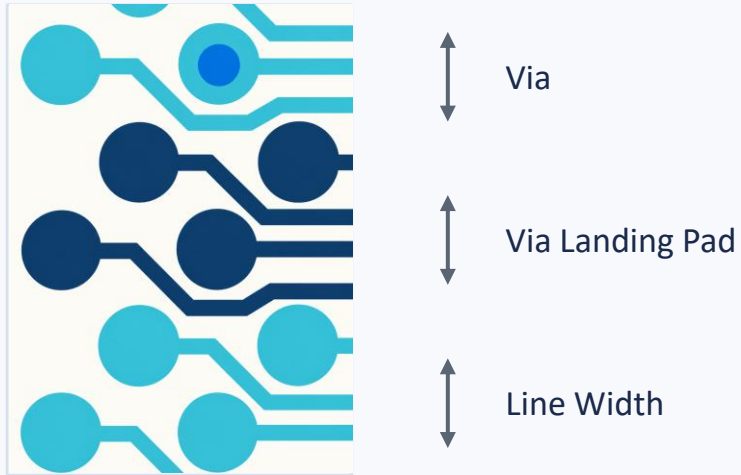


Build-up materials: sub-3 μm line/space feasibility demonstrated

Lithographically Defined Vias Without a Landing Pad

Conventional Build-Up

Laser-defined via with landing pad



Line width $\ll$ via $\ll$ landing pad

Typical industry values: $8\text{--}15\text{ }\mu\text{m} \ll 30\text{ }\mu\text{m} \ll 50\text{ }\mu\text{m}$

Wafer-Level Build-Up

Lithographically defined via — no landing pad



Cross-sectional via array — wafer-level

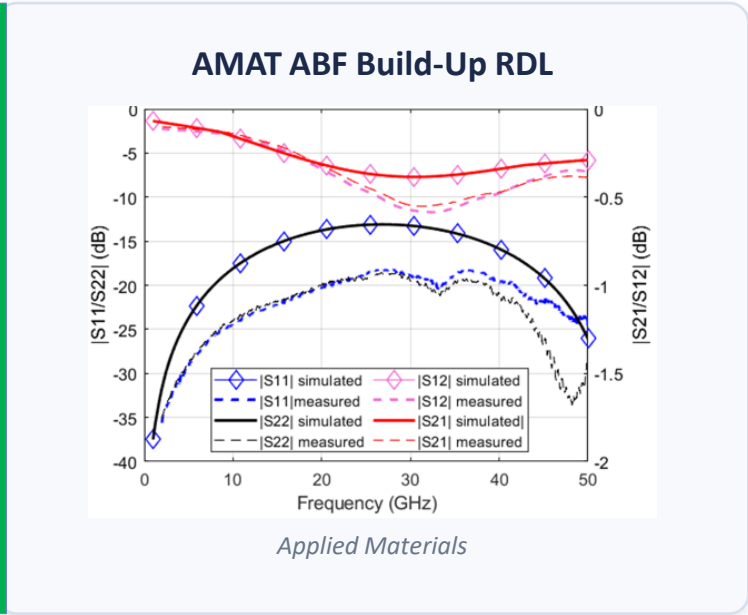
Line width = via = landing pad

Typical value: $5\text{ }\mu\text{m} = 5\text{ }\mu\text{m} = 5\text{ }\mu\text{m}$



Novel lithography-defined vias eliminate the landing pad — via width = line width

Comparison of Wafer-Level: ABF Build-Up vs. Thin-Film RDL (Polyimide) vs. SiO₂/Cu (BEOL) Interconnect

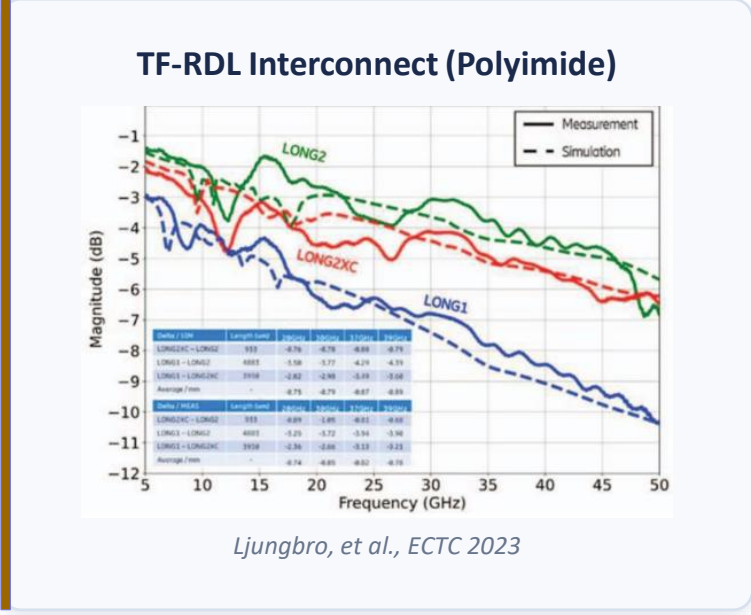


Lowest loss

0.12 dB/mm

@ 40 GHz

20 μ m dielectric — laminated

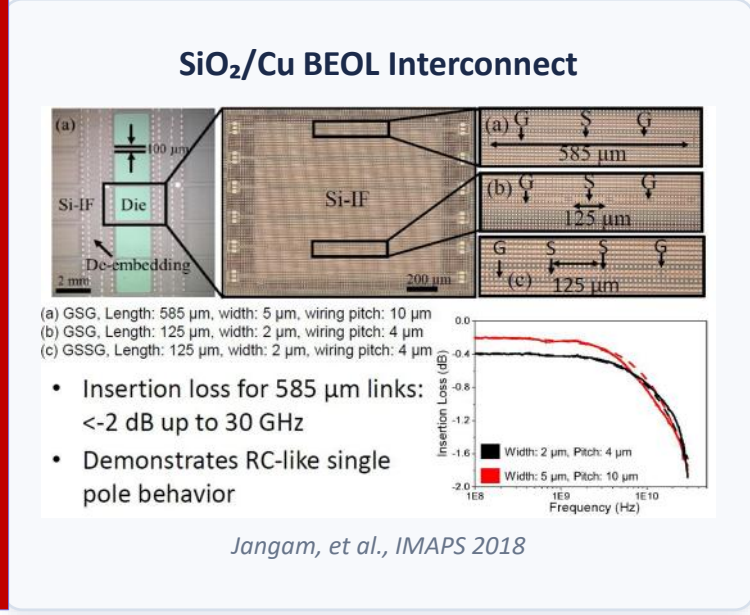


Intermediate

0.8–0.9 dB/mm

@ 30–40 GHz

5 μ m dielectric — spin-on



Highest loss

4 dB/mm

@ 30 GHz

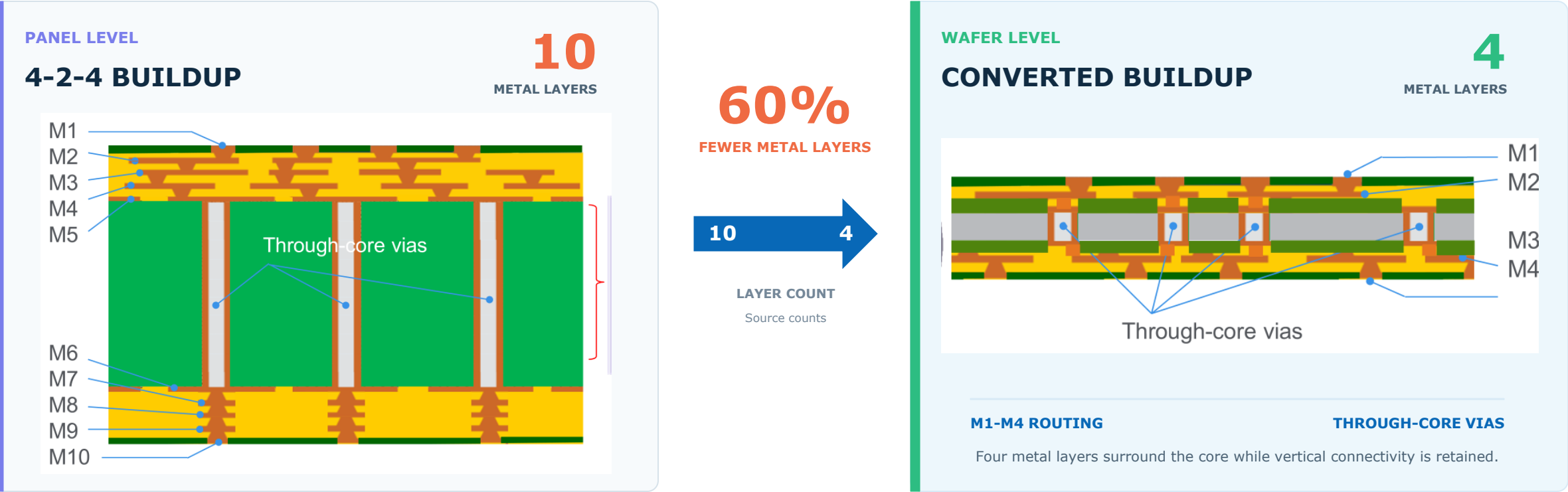
1 μ m dielectric — PECVD

Thicker, low-Dk dielectrics → wider 50 Ω transmission lines → lower RF (conductor) loss



Wafer-level conversion reduces the metal stack from 10 layers to 4

Through-core vias preserve vertical connectivity while the routing structure becomes substantially simpler.



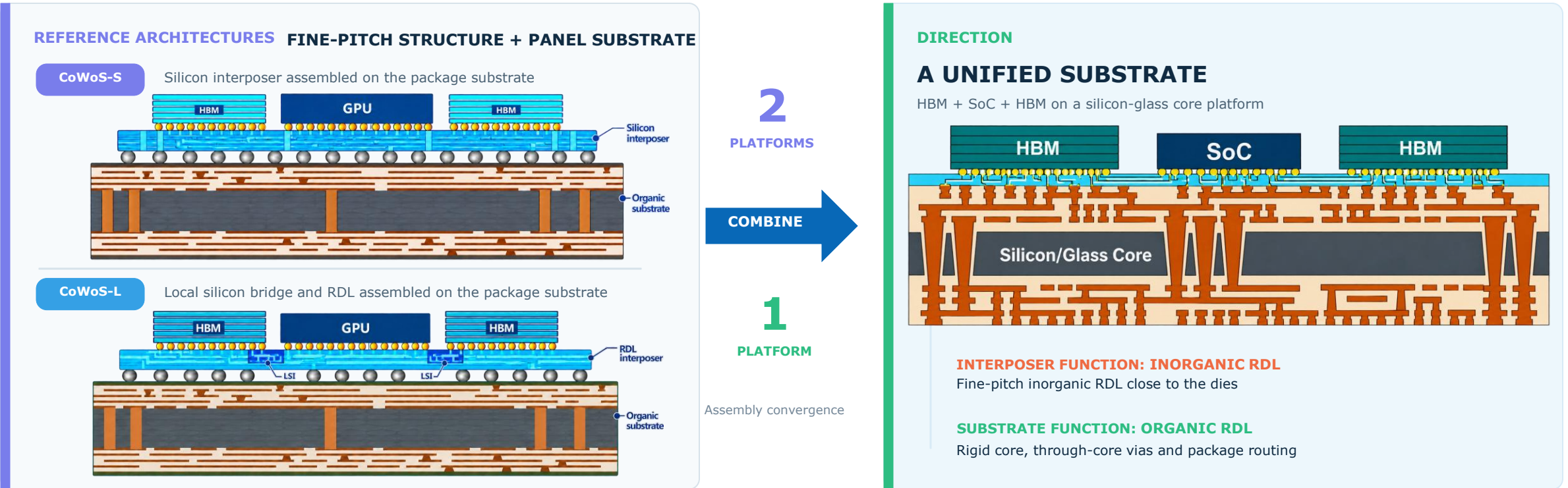
ARCHITECTURAL SHIFT

Wafer-level conversion simplifies the routing stack while retaining through-core connectivity.

The 10-to-4 layer change represents a 60% reduction in metal-layer count; implementation depends on routing and reliability requirements.

One platform combines interposer and substrate functions

The Si/Glass core concept integrates fine-pitch RDL, a rigid core, and package routing without a separate interposer-to-substrate assembly.



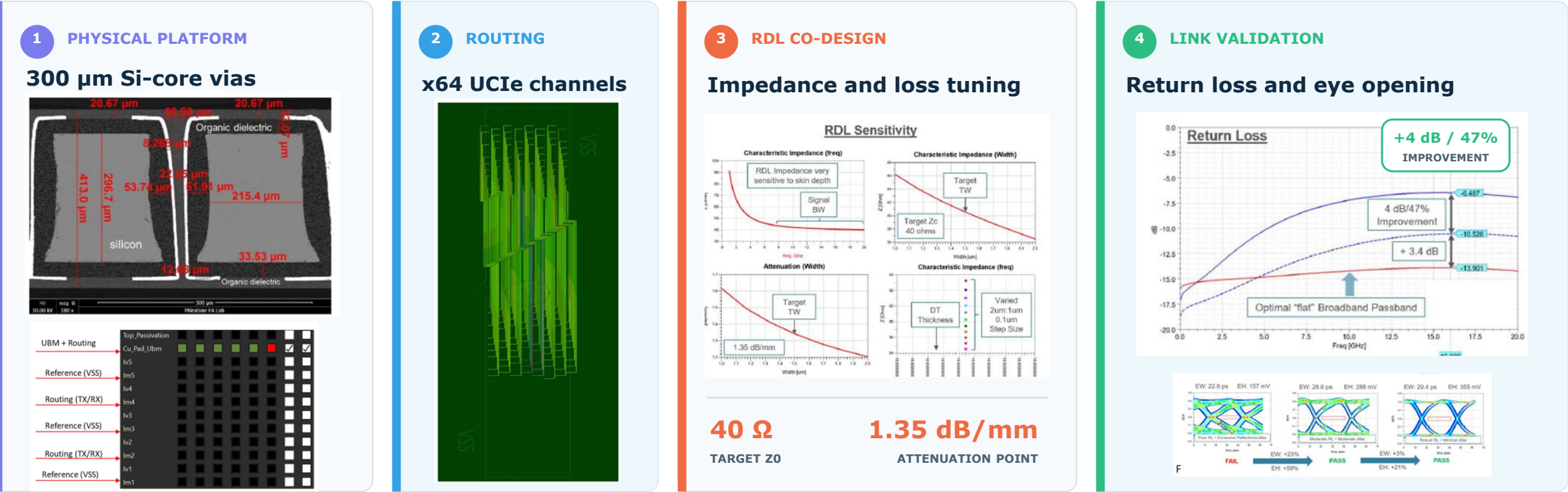
PROCESS INTENT

Move substrate build-up processes to wafer/panel scale and integrate them with wafer-level fine-pitch processing.

This direction aims to eliminate a separate interposer assembly.

Co-designed vias and RDL enable x64 UCIE at 32 GT/s on silicon core

The evidence chain connects the physical stack, parallel routing, RDL sensitivity and link-level signal integrity.



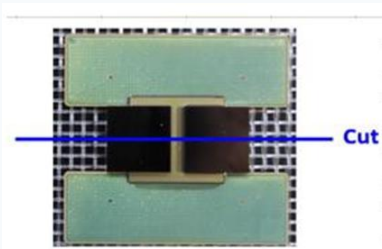
Complete photonic-chiplet assembly on a reduced-layer wafer-level substrate

The process integrates electrical routing, optical access and package formation before the module leaves the wafer or strip flow.

1 ASSEMBLE

Wafer / strip integration

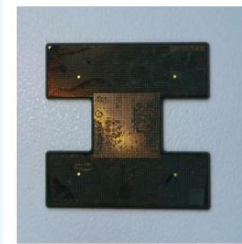
Interconnect the photonic chiplets before package separation.



2 SINGULATE

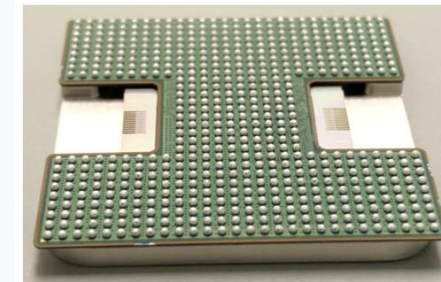
Define the module outline

The cut creates the final photonic-package form factor.



3 COMPLETE

Package-ready photonic BGA



BGA INTERFACE

Electrical connection to the board

OPTICAL ACCESS

Openings preserve access to the photonic interfaces

LAYER-REDUCED CROSS-SECTION

Continuous wafer-level substrate beneath the assembled components

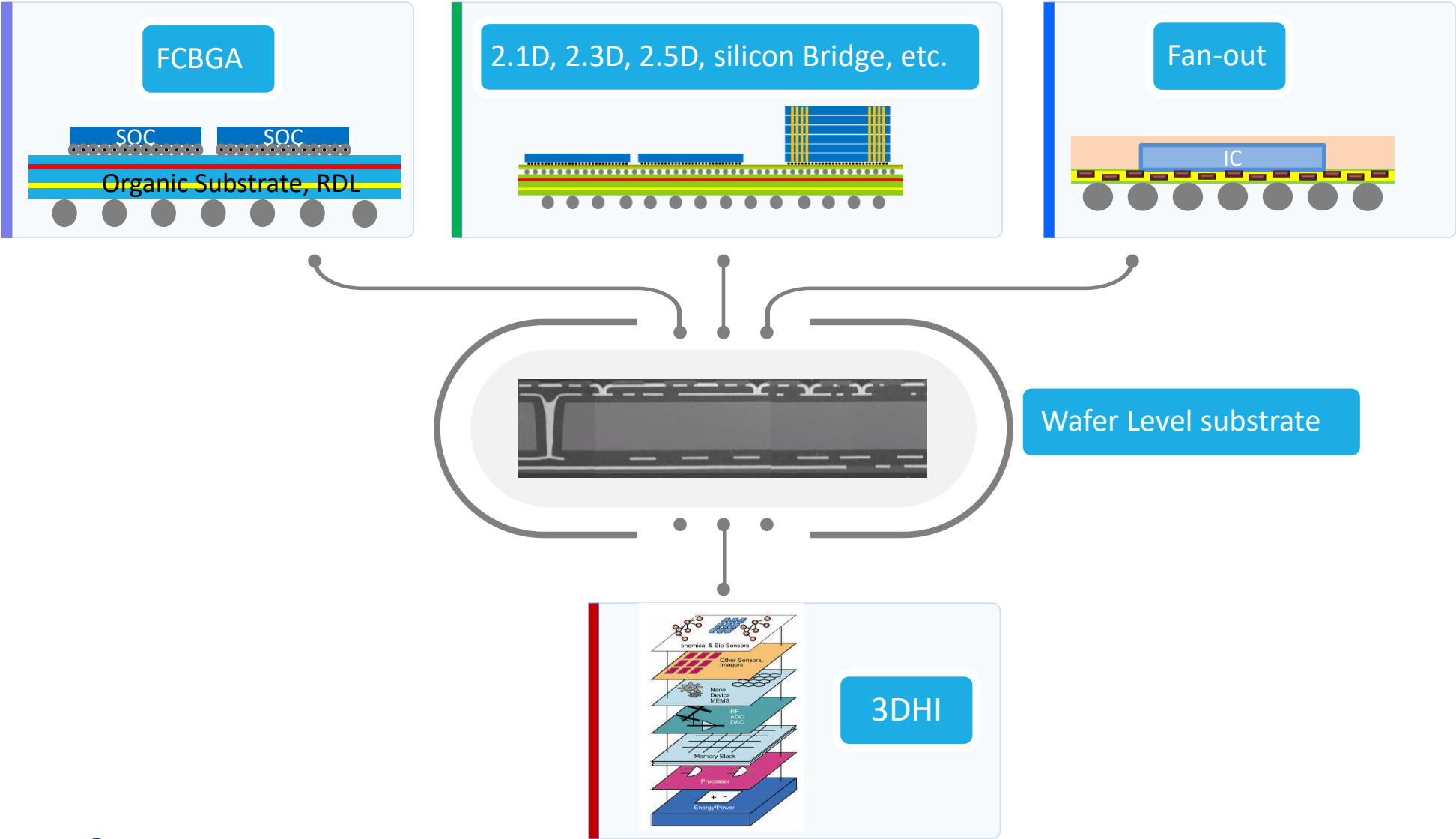


INTEGRATION INTENT

Complete the chiplet assembly on the wafer-level substrate, then singulate a package-ready photonic module.

Layer reduction consolidates the package structure while retaining the electrical BGA and optical interfaces.

CONVERGING TO A COMMON PLATFORM

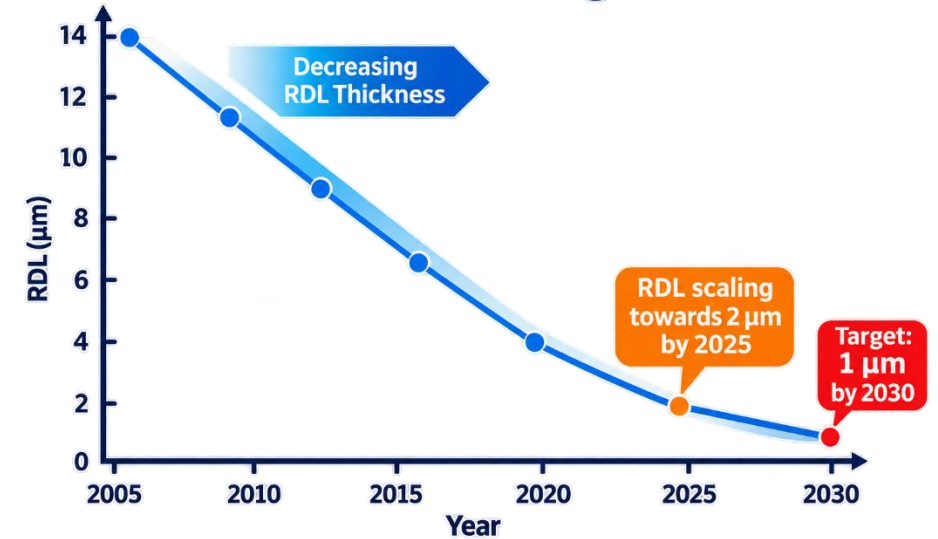
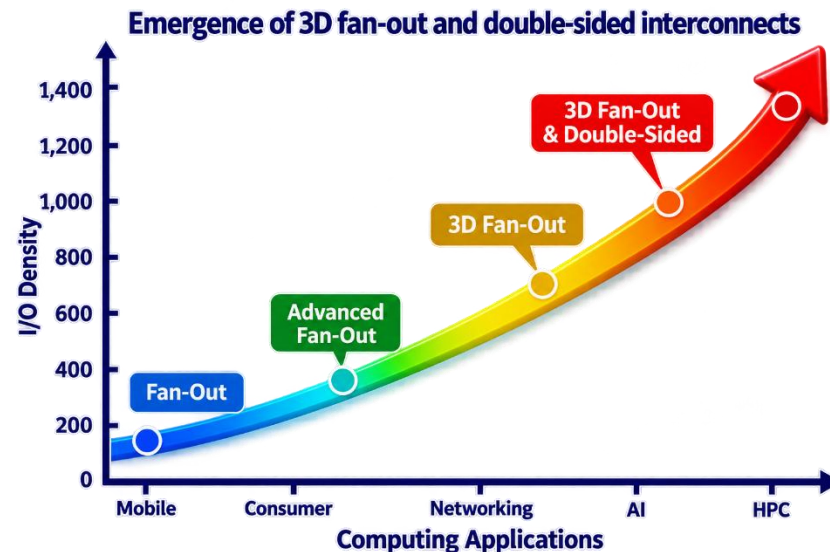


Fan-Out Evolution

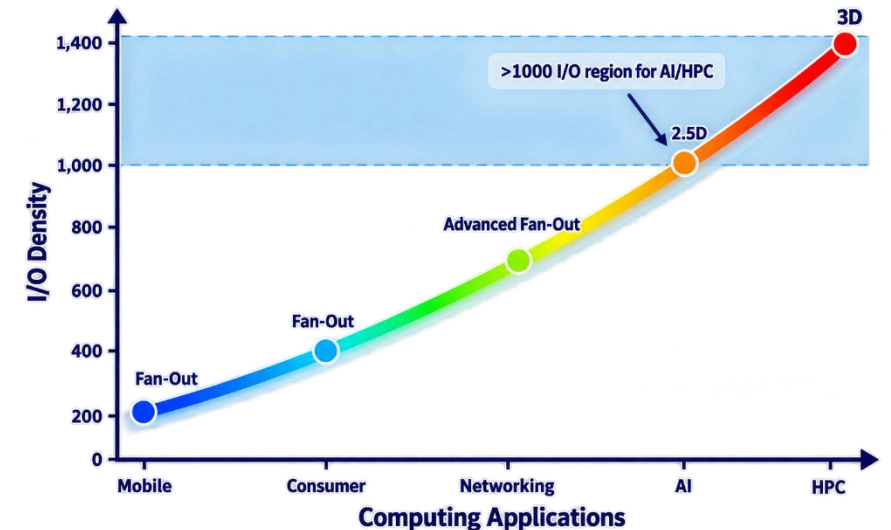
FAN-OUT EVOLUTION

- ⊙ Transition from single-die to multi-die heterogeneous architectures
- ⊙ RDL scaling roadmap: $15\mu\text{m} \rightarrow 5\mu\text{m} \rightarrow 2\mu\text{m} \rightarrow <1\mu\text{m}$ (future)
- ⊙ Enables higher I/O density and improved electrical performance
- ⊙ Increasing I/O density (>1000) for AI/HPC applications
- ⊙ Emergence of 3D fan-out and double-sided interconnects

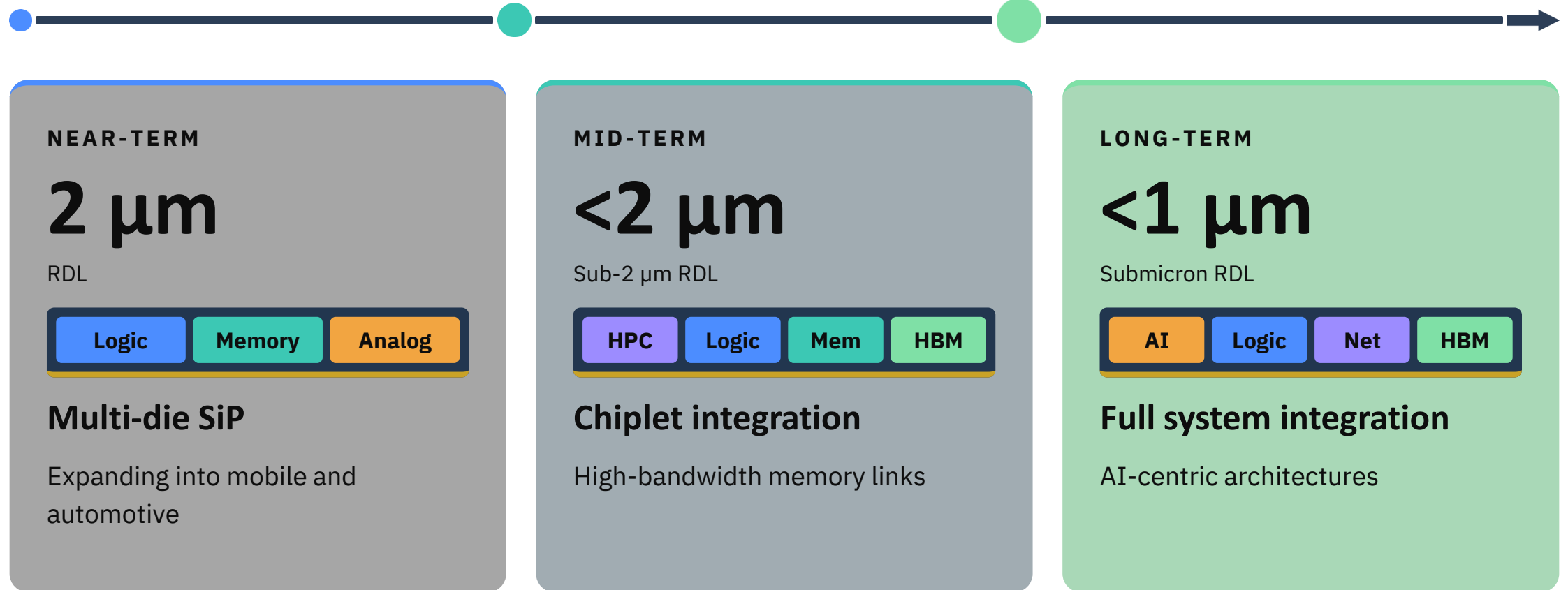
Fan-Out RDL Scaling Trend



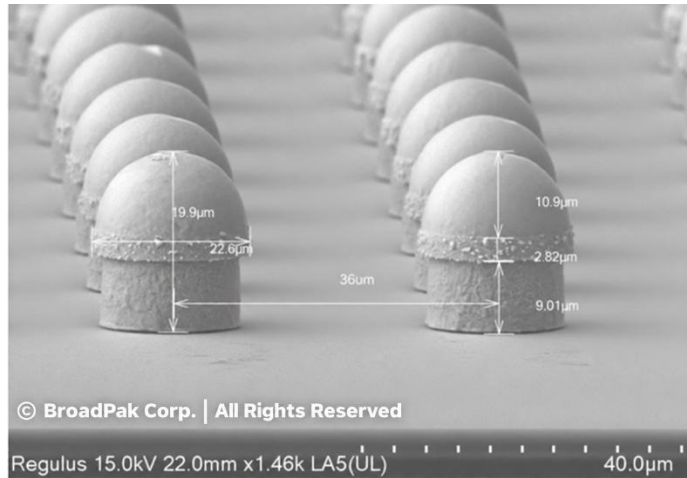
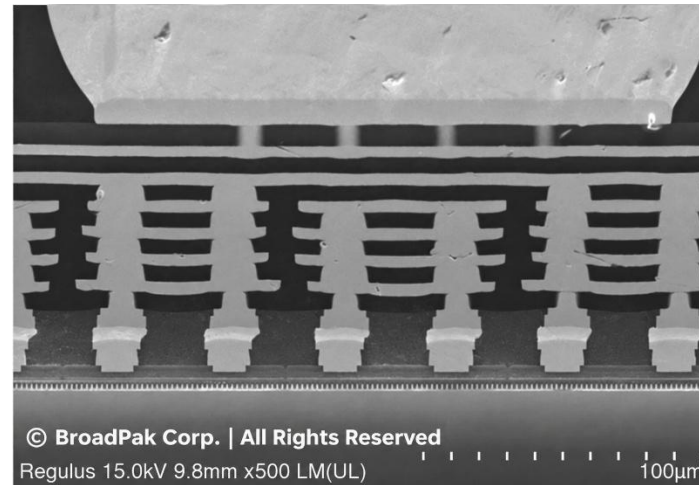
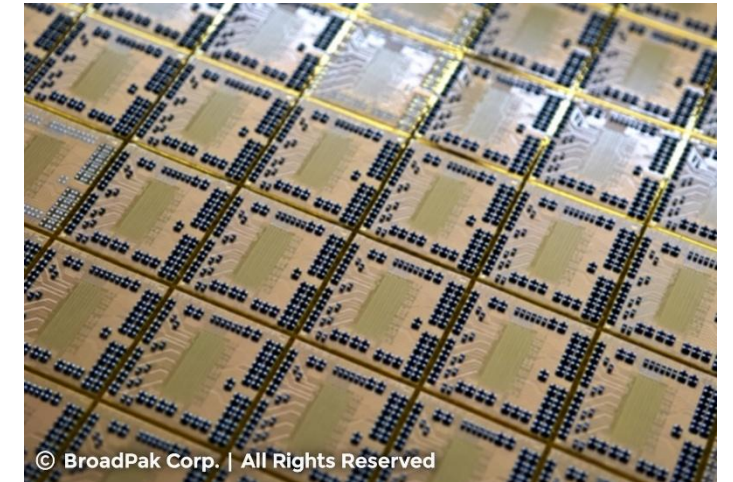
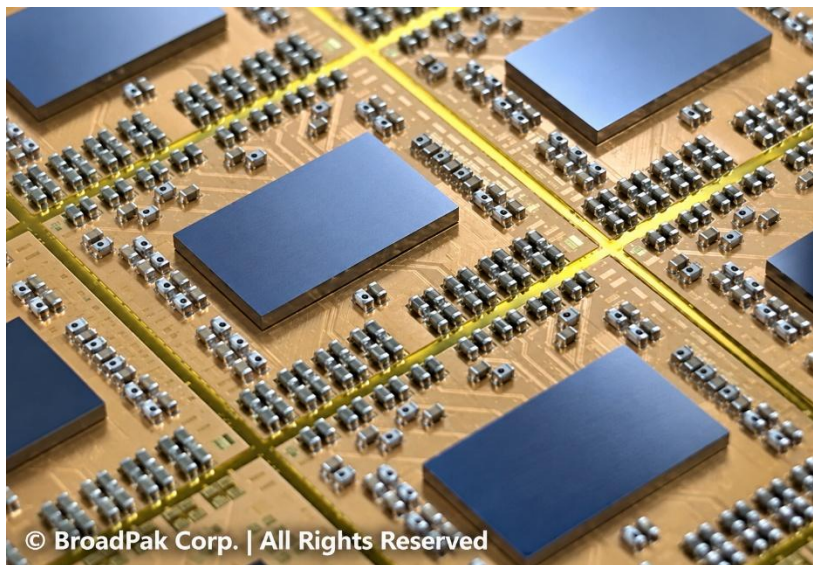
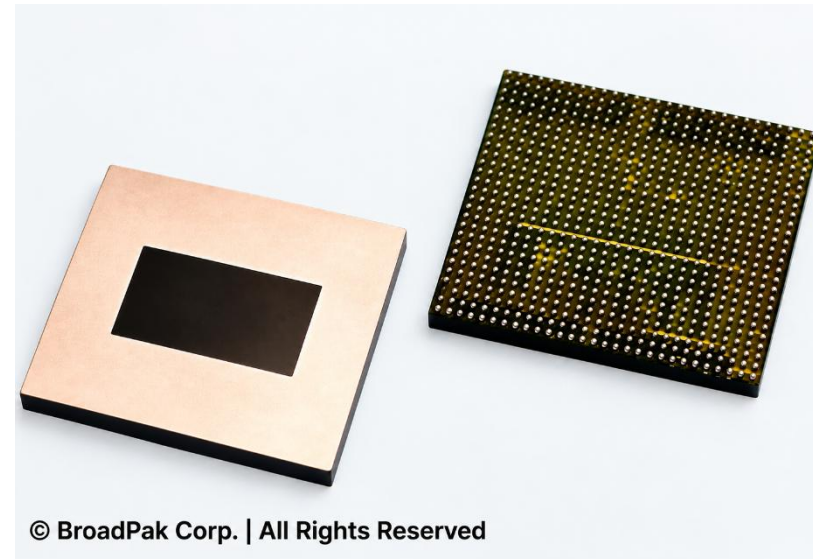
I/O Density vs Computing Applications



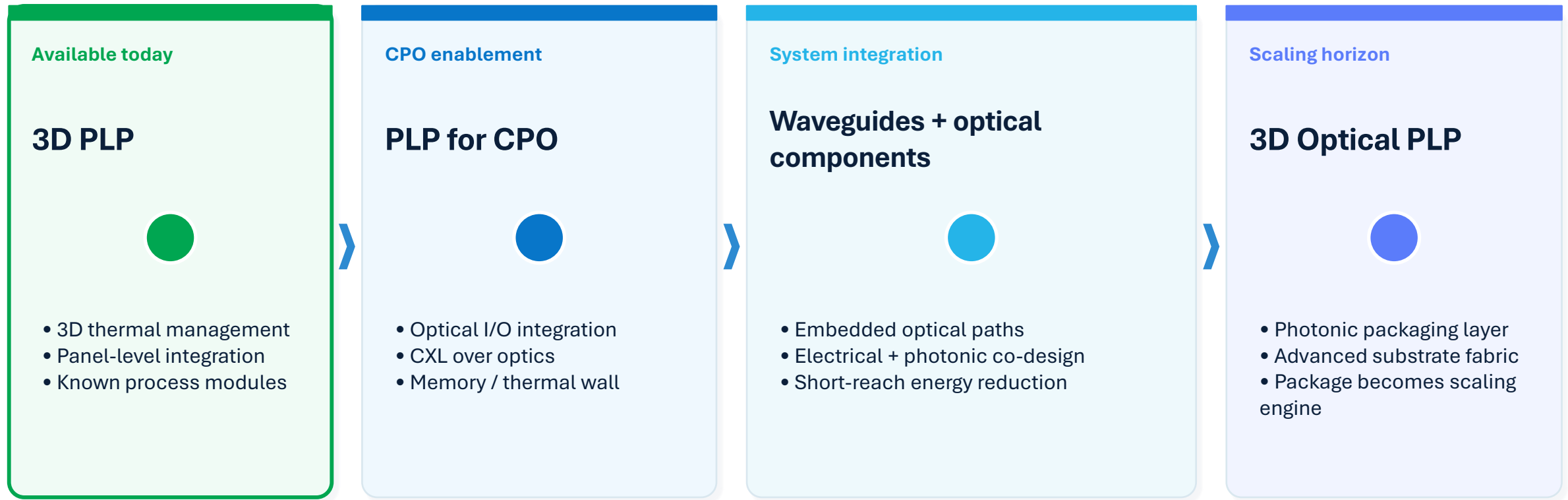
ROADMAP: FINER RDL, BIGGER SYSTEMS



BROADPAK 7P7M WLP | QUALIFIED | PRODUCTION



Packaging innovation becomes equal to front-end scaling



Key message: the package becomes the scaling platform for memory bandwidth, thermal density, optical I/O, and AI fabric integration.

Summary

Advanced substrates define the scaling envelope for AI infrastructure.

01

AI scaling pressure is moving into the package

Models, context windows and KV-cache growth push bandwidth, capacity, latency, power and interconnect together.

02

The substrate becomes the system fabric

It carries chiplets, HBM, CXL/UALink reach, optical I/O, and the thermal/power structure that keeps accelerators productive.

03

Materials set the practical roadmap

Organic remains the volume workhorse; glass and silicon-core extend rigidity, body size, CTE matching and fine routing for higher-end systems.

04

Direction: wafer-level, fan-out and photonics

Reduced-layer WLS, Si-core co-design, 3D PLP and CPO-ready platforms move packaging closer to system-level scaling.

Key message

Packaging innovation is becoming equal to front-end scaling

Advanced substrates are the foundation for scale-in, scale-up, scale-out and optical AI infrastructure.

Thank You