



Overcoming the Scale-Out Energy Penalty

Co-Packaged Photonics Meets Glass Microfluidics

Nilesh Kamdar
General Manager, Keysight EDA

From the “OG” of Silicon Valley to Today



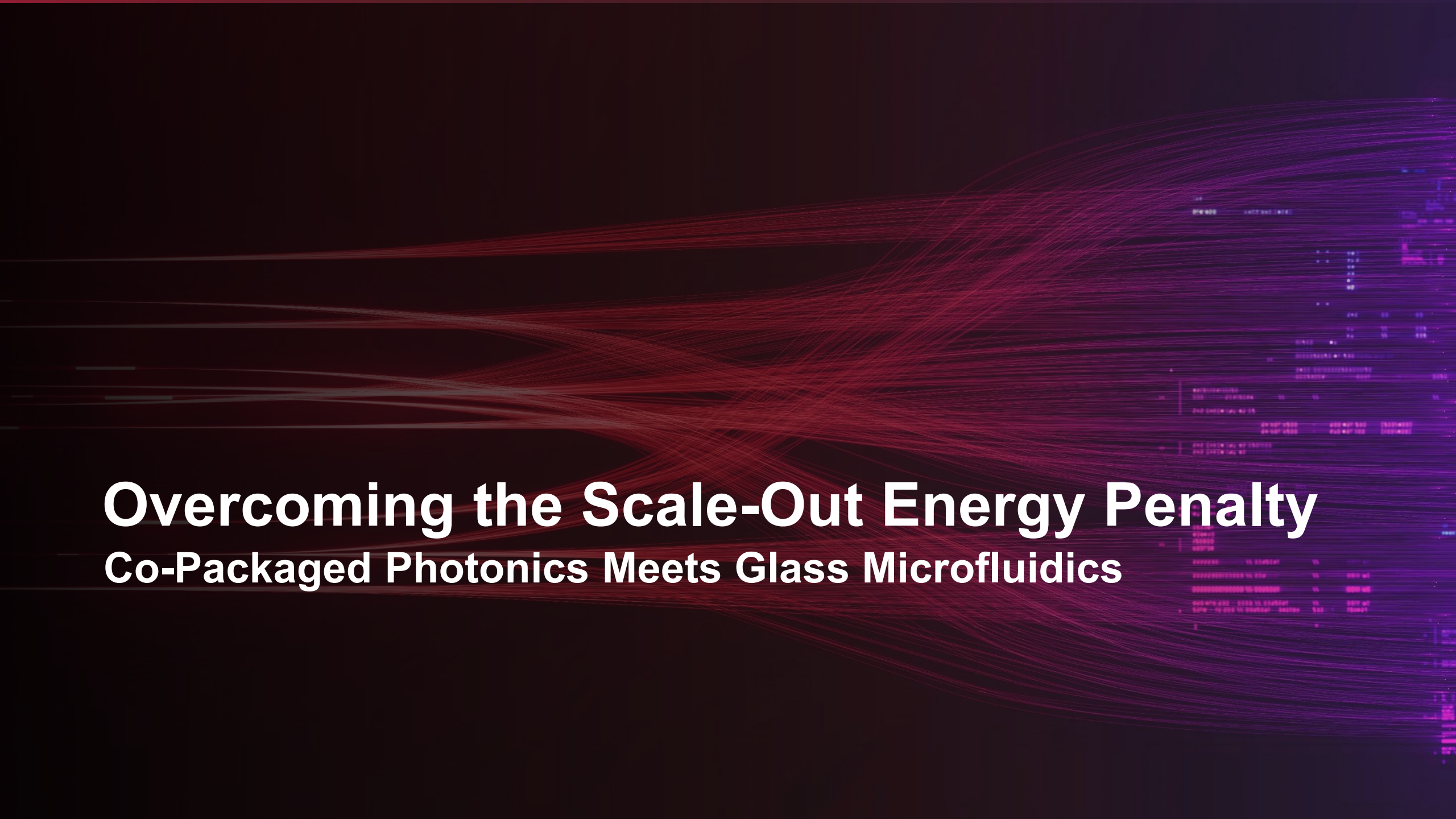
**40+ years of innovation
in EDA**



**25 years at Keysight EDA
Partnerships & Collaboration**

Keysight EDA Software

First by Design



Overcoming the Scale-Out Energy Penalty

Co-Packaged Photonics Meets Glass Microfluidics

Copilot

+ Where is this query being executed?



AI-generated content may be incorrect

The precise location where this query was executed is not exposed to me. It was processed within Microsoft-managed cloud infrastructure, but I cannot determine the specific region or datacenter for this individual interaction.

microsoft +1



Microsoft's New Wisconsin Datacenter Campus



Rows of GB200 Rack Systems



Rooftop Closed-Loop Liquid Cooling

GIGABYTE + NVIDIA GB300 NVL72



Management Switches

- 2 x OOB management switches
- 1 x Optional OS switch

3 x 1U 33kW Power Shelves

10 x Compute Trays

- 1U XN15-CB0-LA01

9 x NVIDIA NVLink™ Switch Trays

- 1U NVLink Switch tray
- 144 x NVLink ports per tray
- Fifth-generation NVLink with 1.8TB/s GPU-GPU interconnect

8 x Compute Trays

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3 x 1U 33kW Power Shelves

Compatible with in-rack CDU or in-row CDU

GIGABYTE + NVIDIA GB300 NVL72



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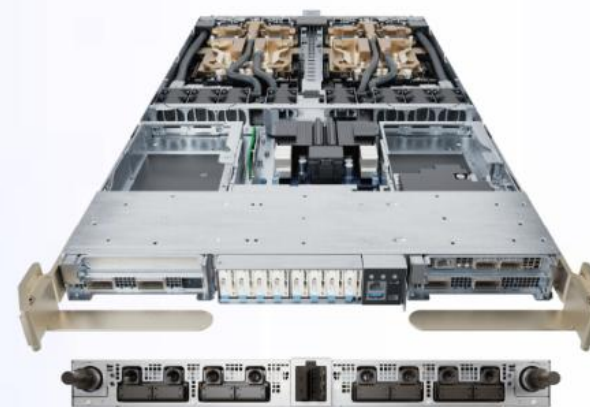
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Compatible with in-rack CDU or in-row CDU

The Age of AI reasoning. Denser compute, faster interconnects, more power



Compute Tray

Total Rack:

- 76 GPUs & 36 Arm CPUs
- Up to 20TB HBM3E GPU memory
- Up to 198kW of Power
- 72x NVIDIA Connect-8 800G OSFP Ports

GIGABYTE + NVIDIA GB300 NVL72



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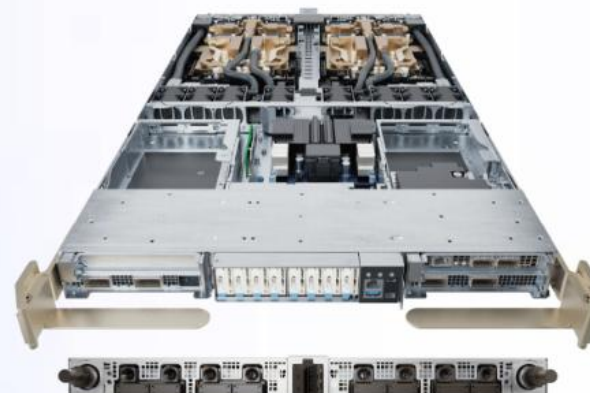
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The Age of AI reasoning. Denser compute, faster interconnects, more power



Capability?

Claude Opus ~5 Trillion parameter model + context =
2 Inference Models per rack system

Claude Sonnet ~1 Trillion parameter model + context =
8 Inference Models per rack system

**So that's inference.
What does it look like for training?**

16x to 20x more resources

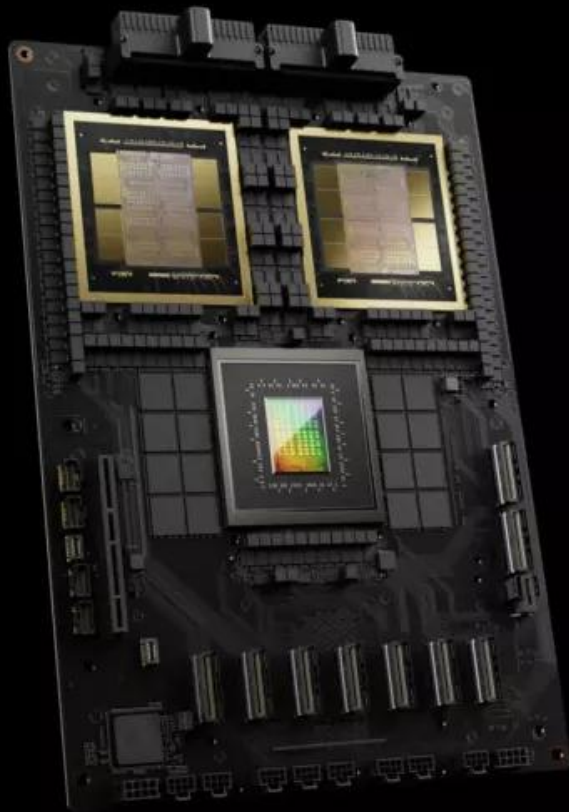
The Future of AI compute is both Denser & Faster

Two major challenges:

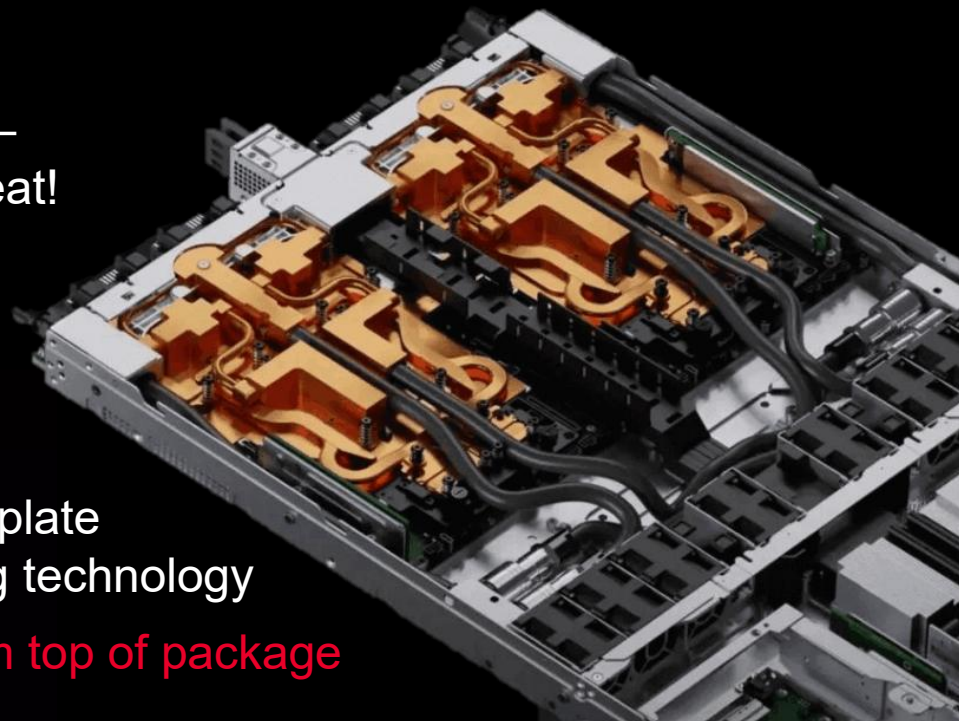
Thermal

Interconnectivity

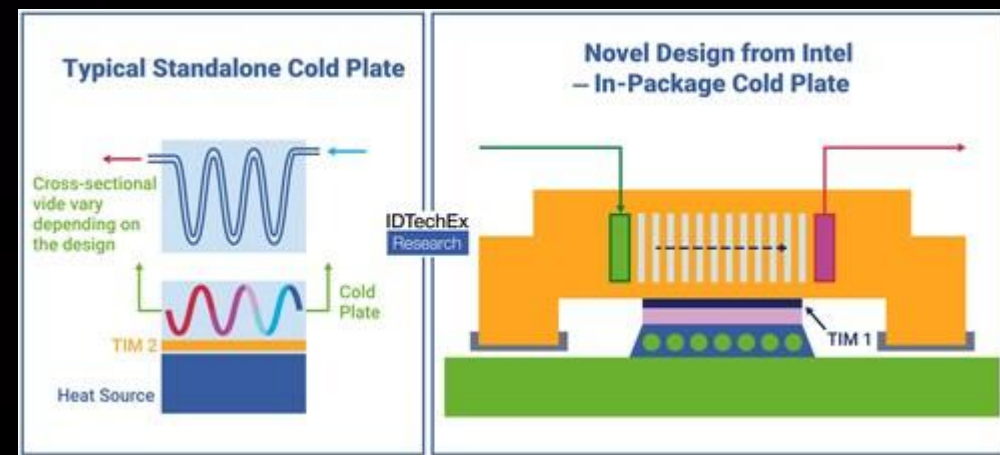
To avoid scale-out –
we can continue to scale up –
but we need to deal with the heat!



NVIDIA Grace Blackwell Ultra Superchip
2 GPUs + 1 ARM CPU



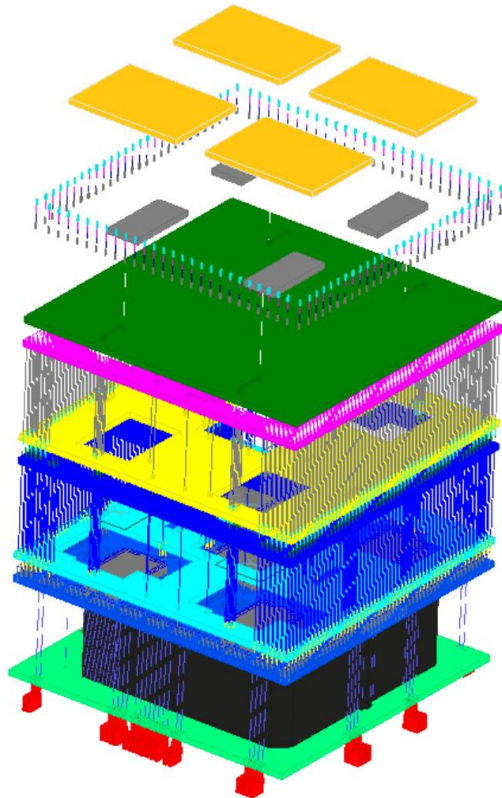
Cold plate
liquid cooling technology
Heat pulled from top of package



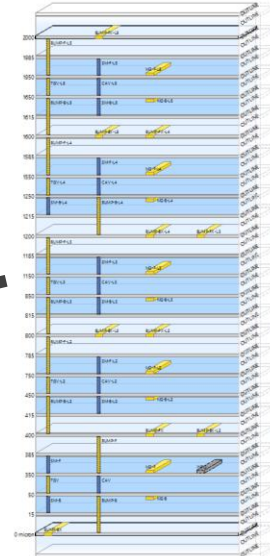
Intel proposed in-package cold plate c.2023
Heat pulled from inside package

Introducing 3D Glass Solutions' Innovative Technology

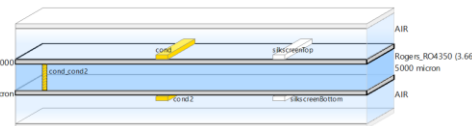
Example of a 3D heterogeneous integration assembly of 5 (photo-sensitive) glass interposer layers. Designs are stacked together forming substrate definitions that can be used for both EM and Thermal analysis.



3DHI RF Assembly in Keysight ADS



5 Glass Layers Stacked on top of the board



Board substrate



Pure Play
Glass Foundry

Glass substrates for
AI Datacenter Applications

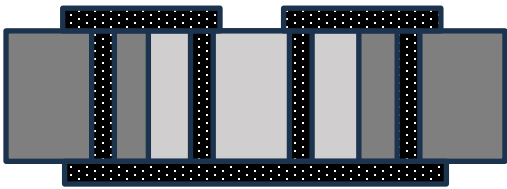
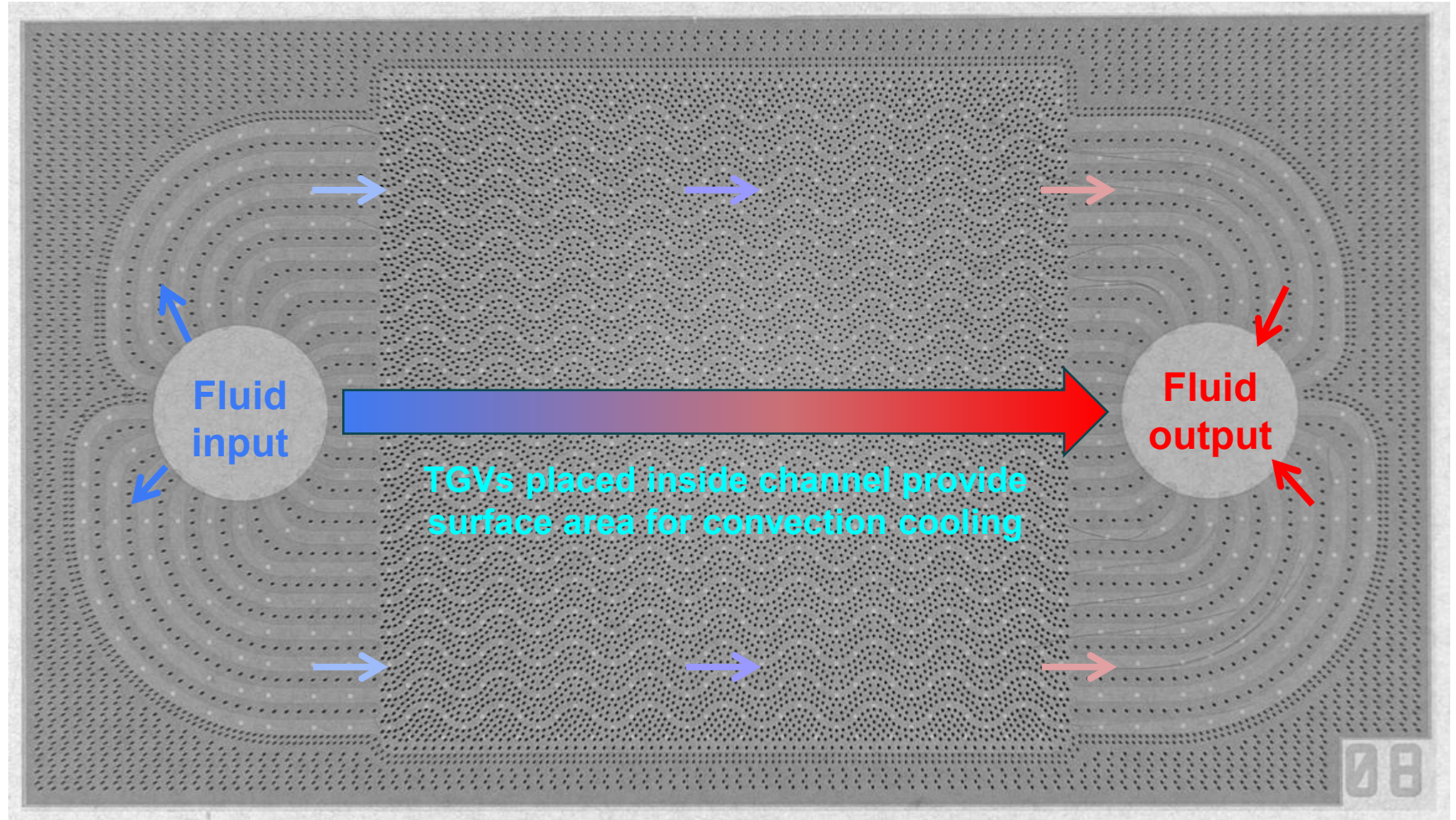


Microfluidic Cooling Substrate

Xray view of microfluidic cooling channel

20 glass channels connecting to each fluid port to evenly distribute fluid across entire device

Copper TGV
Glass
Cooling channel
Etch release holes

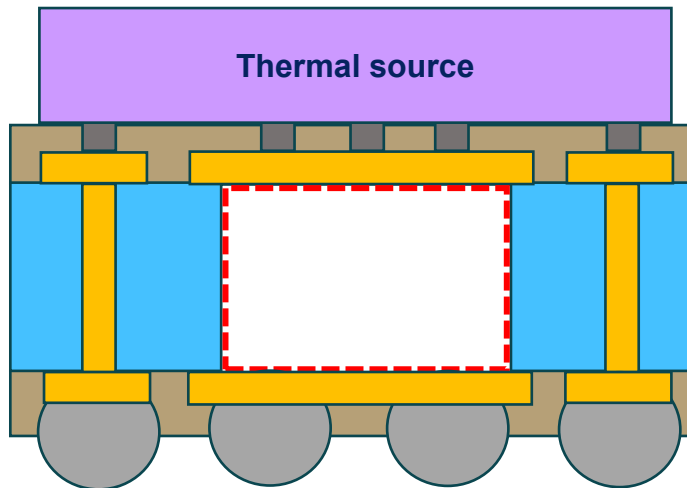


Cooling channel = 8mm x 8mm

Microfluidics Benefits

Using copper TGVs inside cooling channel we can increase thermal transfer area by 25x!

Traditional Fluid Cross-Section



$$Q = U A \Delta T$$

Q = heat flow
U = thermal transfer coeff
A = area
T = temp difference

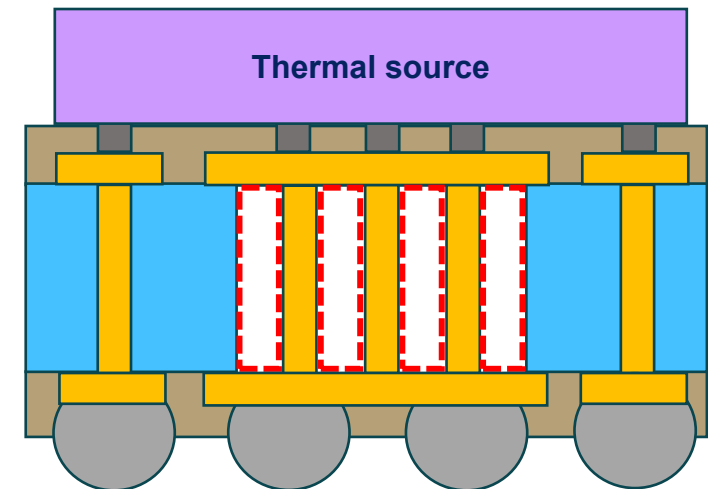


Thermal transfer area



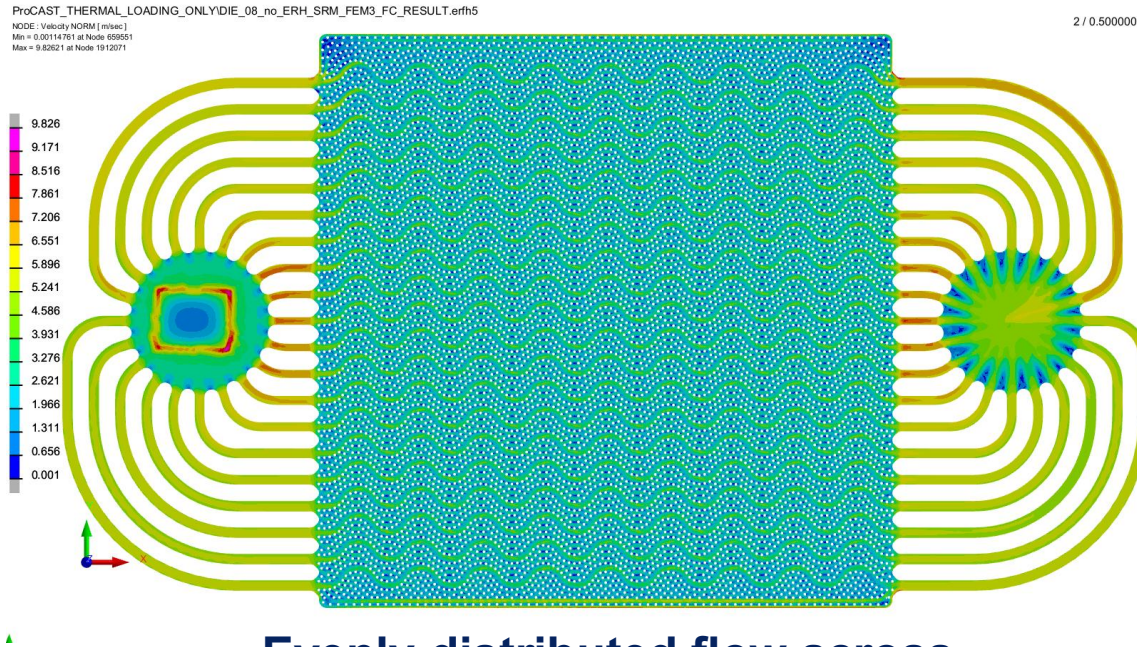
Area increased by 25x

3DGS Fluid Cross-Section (incorporate TGVs in fluid path)



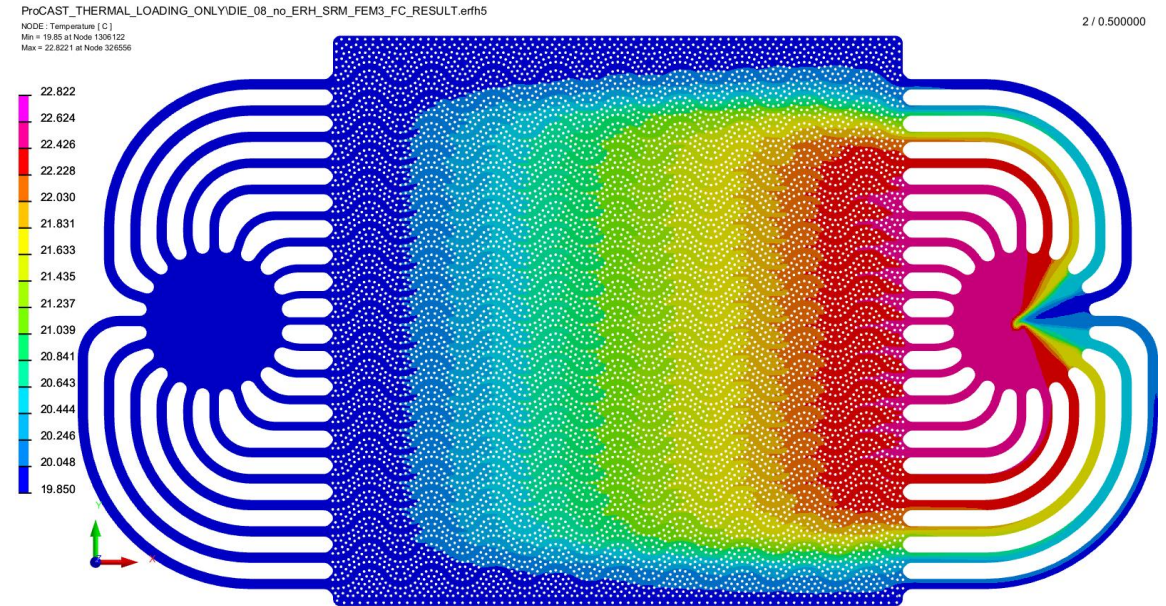
CFD Simulation Results

Fluid velocity [m/s]



**Evenly distributed flow across
width of channel @ 50 psi
Flow rate (meas): 227 mL/min
Flow rate (sim): 232 mL/min**

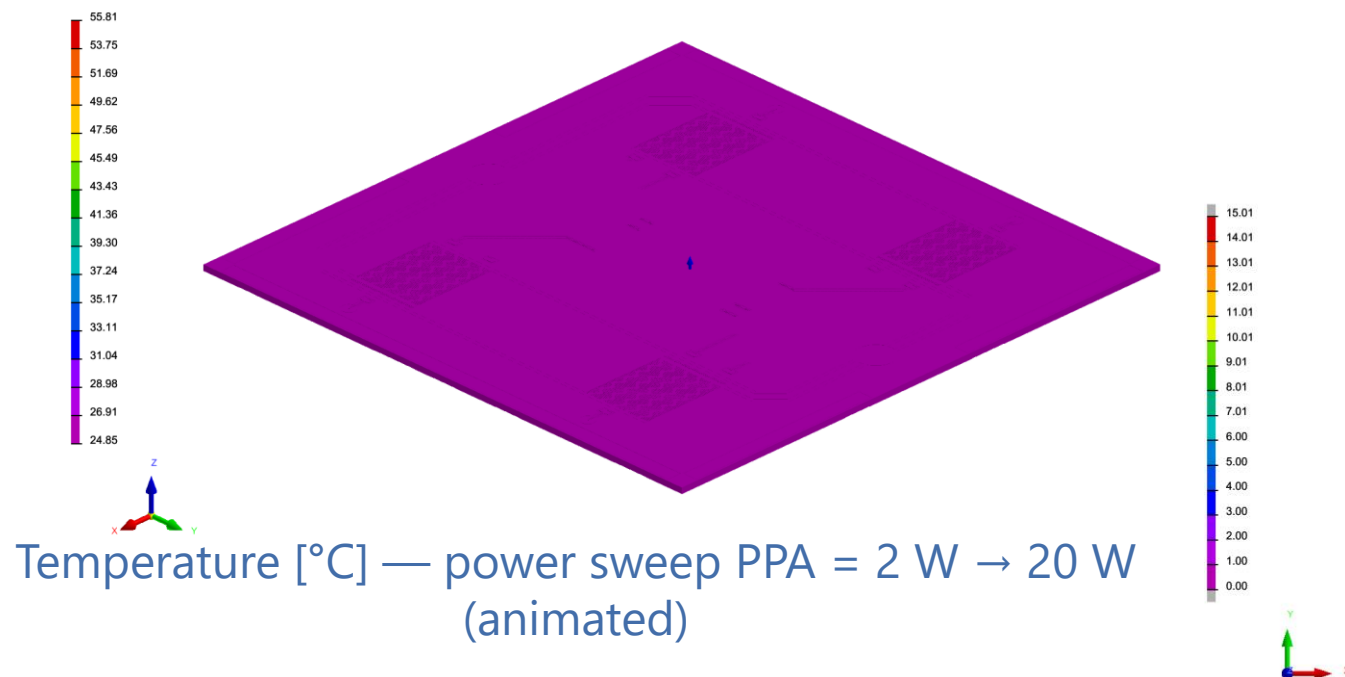
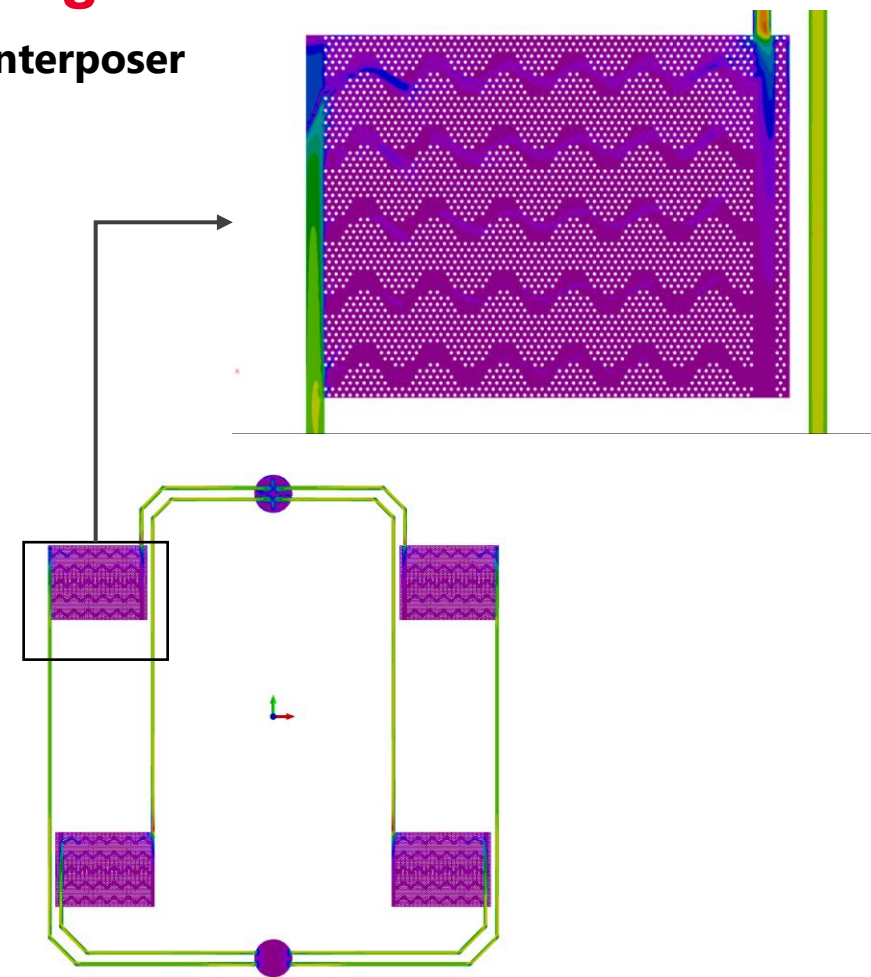
Fluid temperature [°C]



**Top side of substrate with 40W
thermal load applied (<3°C rise)
Delta T (meas): 2.9°C
Delta T (sim): 2.3°C**

Pushing 10x Power Output with Microfluidic Cooling

Heat extracted directly from chips through liquid cooling inside the glass interposer



Fluid velocity [m/s]

Same space -> More Power -> Microfluidic Cooling -> Stable temperature

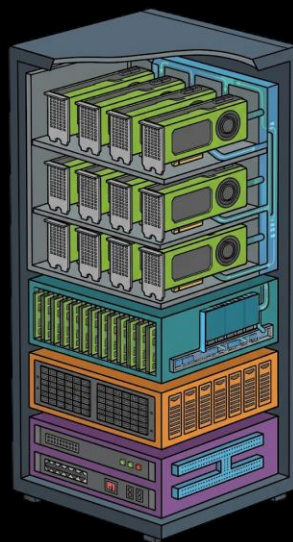
The Future of AI compute is both Denser & Faster

✓ Two major challenges:

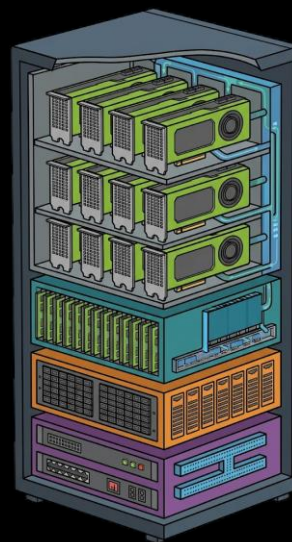
Thermal – Novel liquid cooling – Well funded glass foundry
Interconnectivity

Scale Up ✓

Scale Out ?

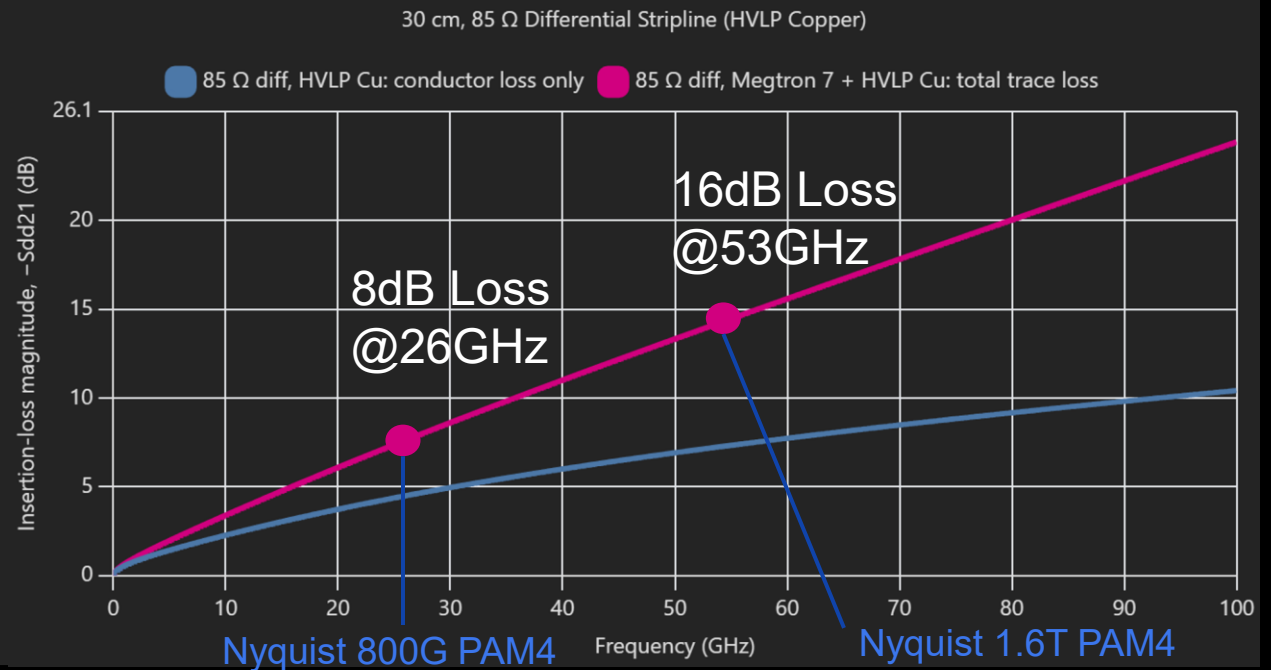
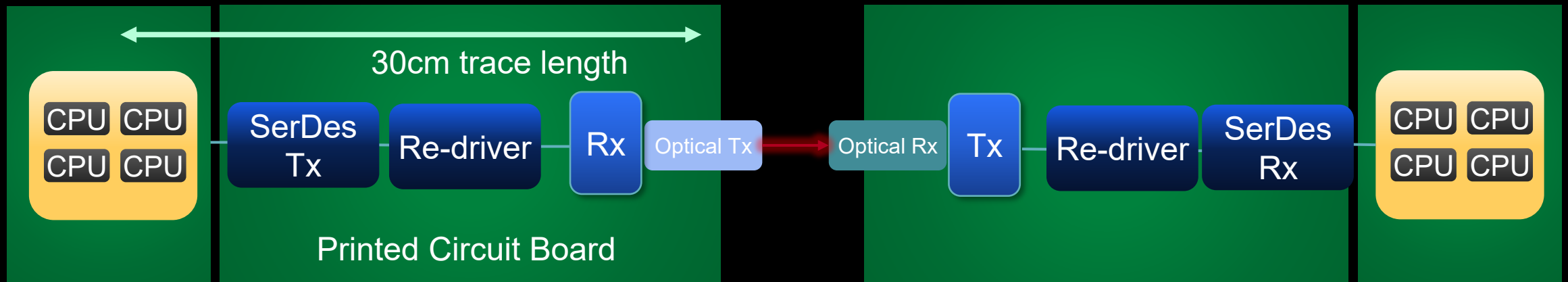


800G DR8
Single Mode
Fiber
Up to 500m



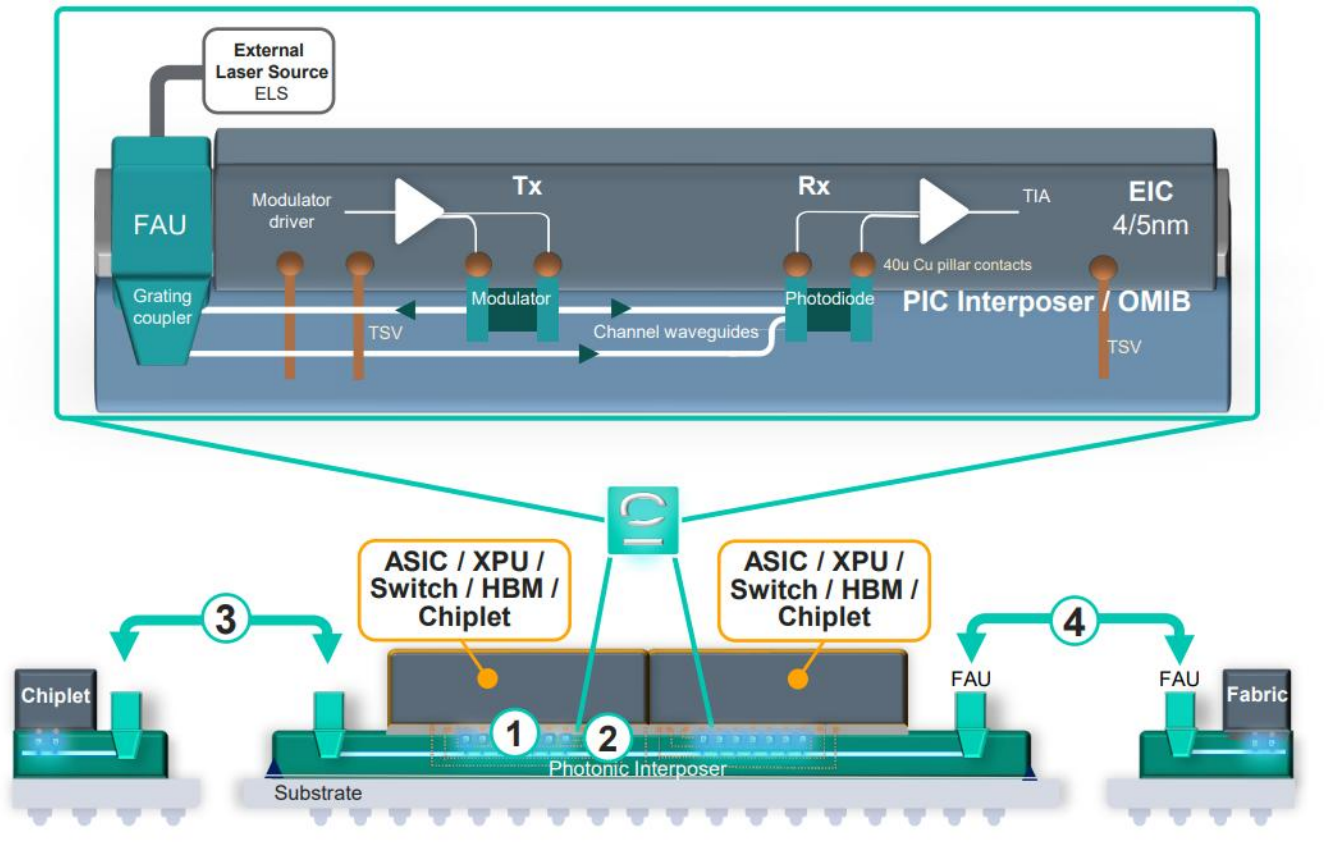
The Scale-Out Energy Penalty:

>50% of Interconnect Power Consumed by SerDes DSPs just to get to the optical link

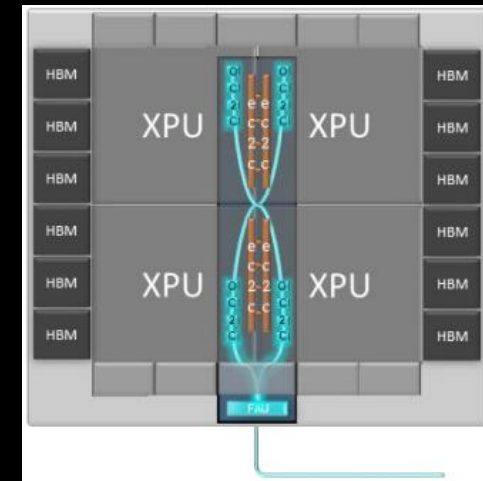


Avoiding the Scale-Out Energy Penalty:

Co-Packaged Optics With Silicon photonics Interposers

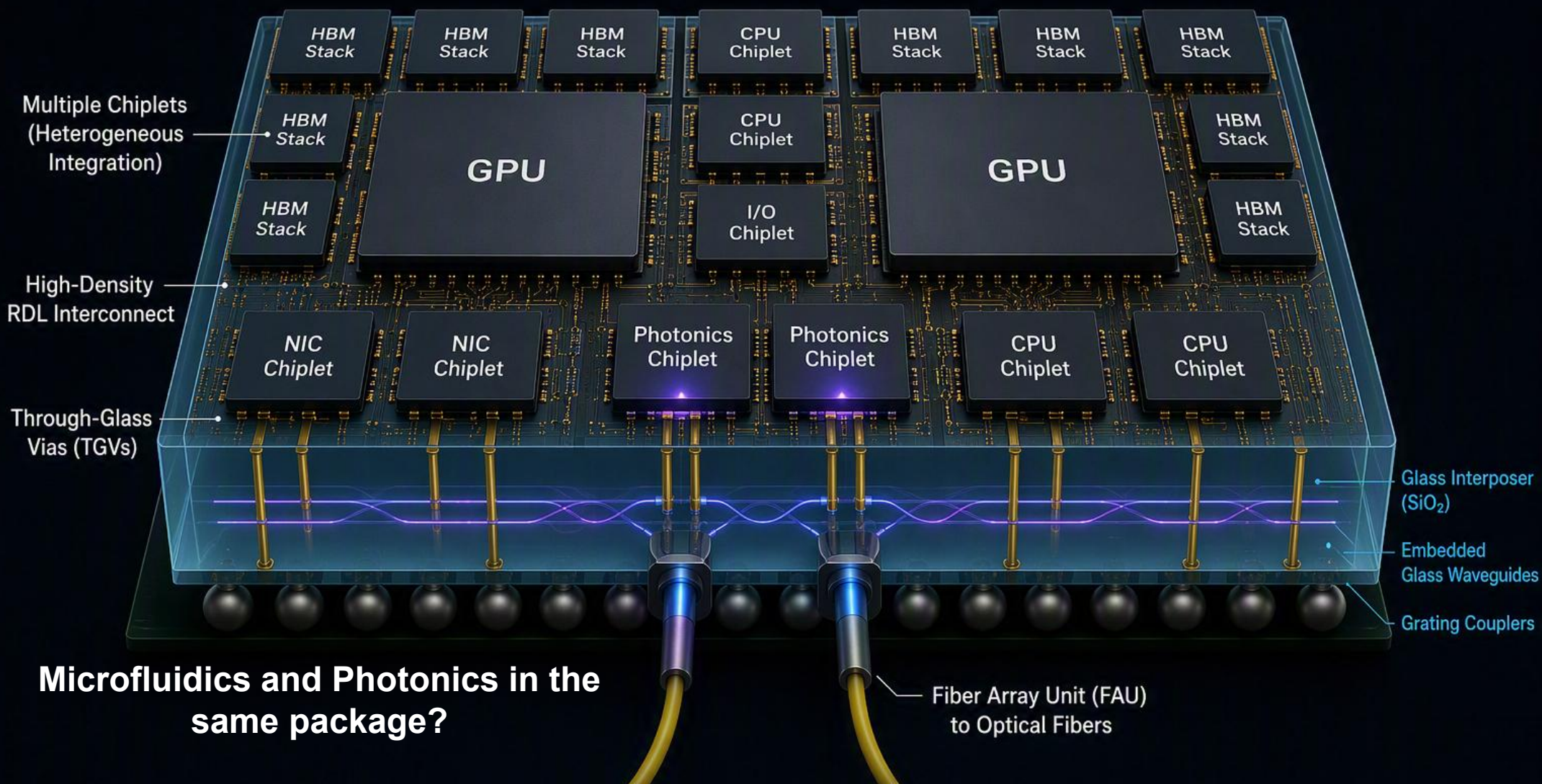


Source: 'Marvell to acquire Celestial AI' investor disclosure, Dec 2025



1. Within Chip
2. Within Package
3. Package-to-Package
4. Package-to-Fabric

GLASS INTERPOSER FOR PHOTONICS APPLICATIONS



**Many opportunities to solve these
design and workflow challenges.
What is the **Keysight** approach?**

Managing Complexity with Engineer-led Multi-Domain Exploration

SI

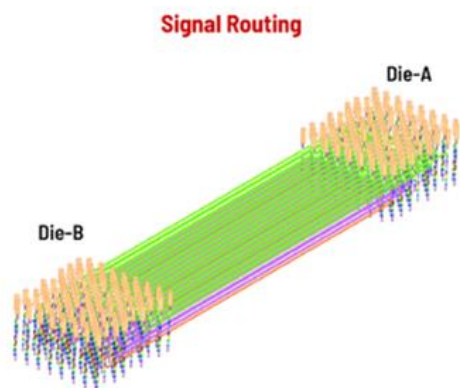
PI

Optical

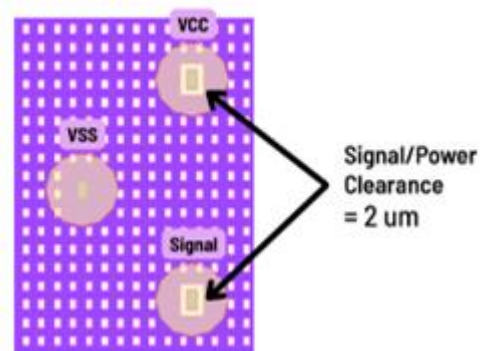
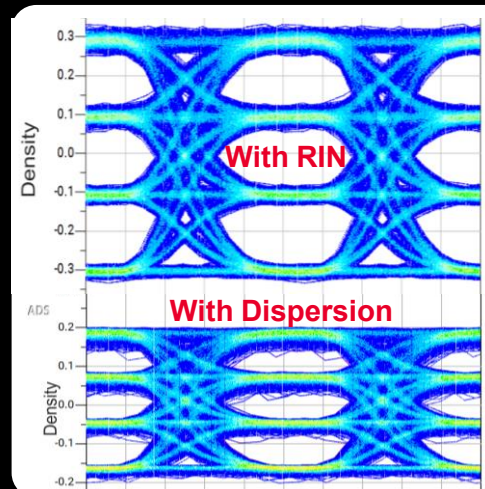
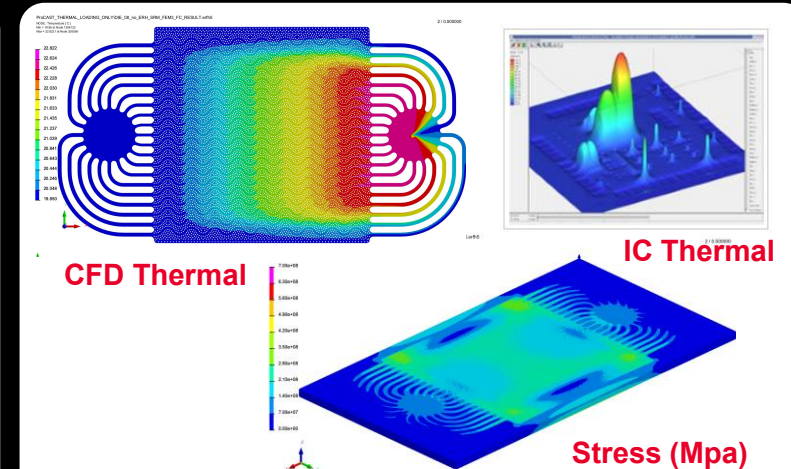
Thermal

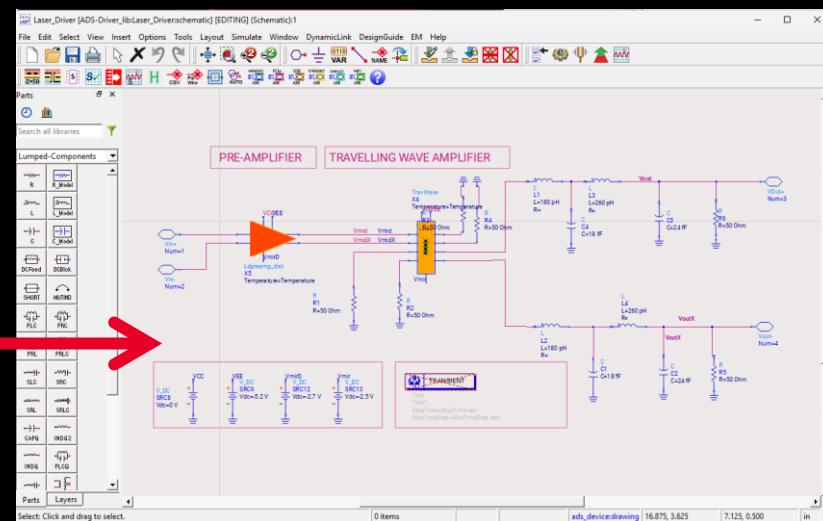
Stress

Automated UCIe Die-to-Die Routing with LLM



Net-Aware Hatch Ground



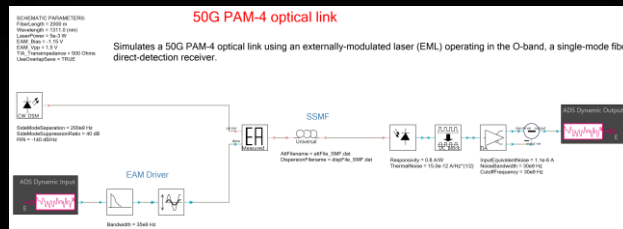
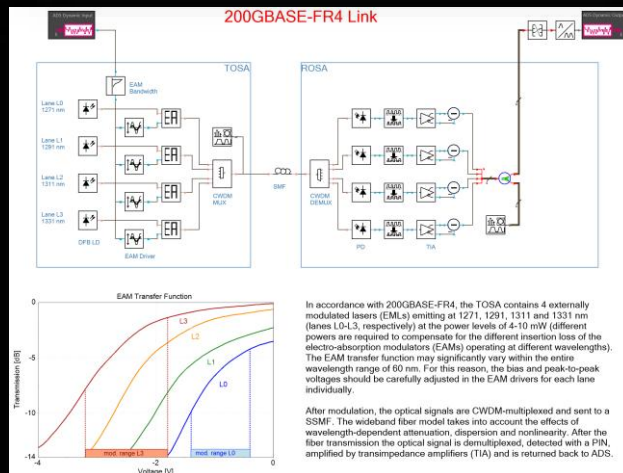
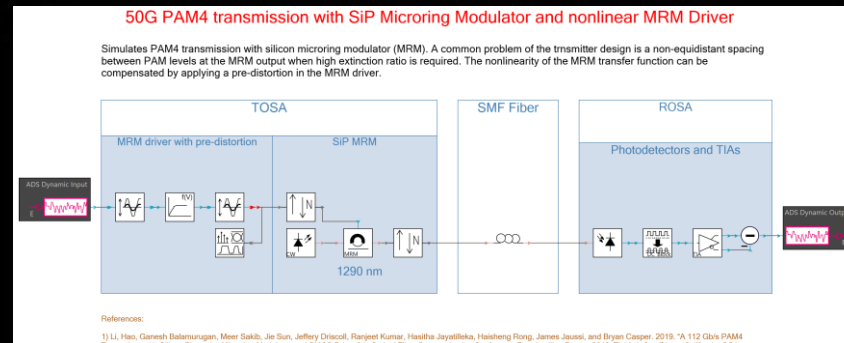
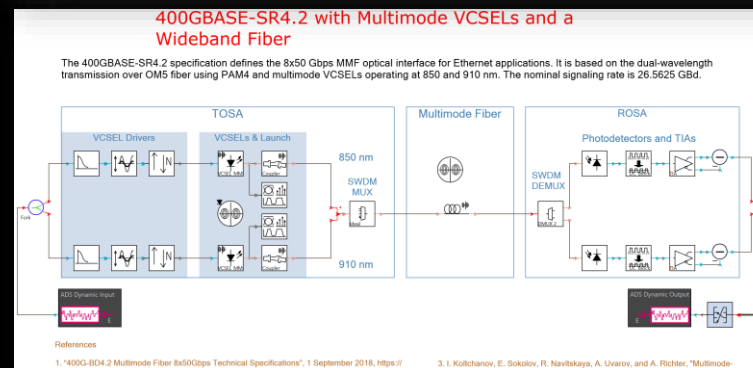
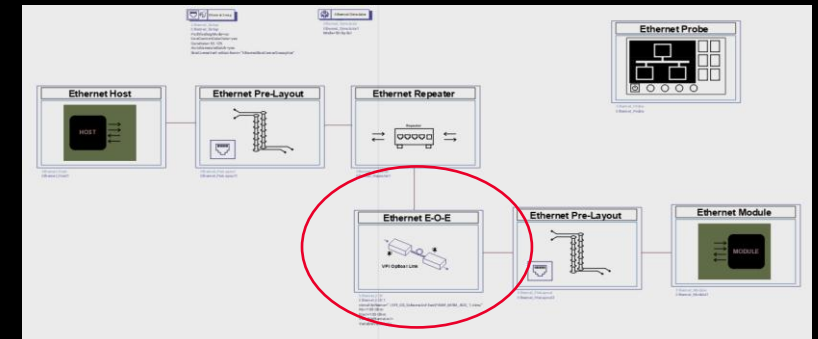


Co-sim: VPI <-> ADS CE/Tran

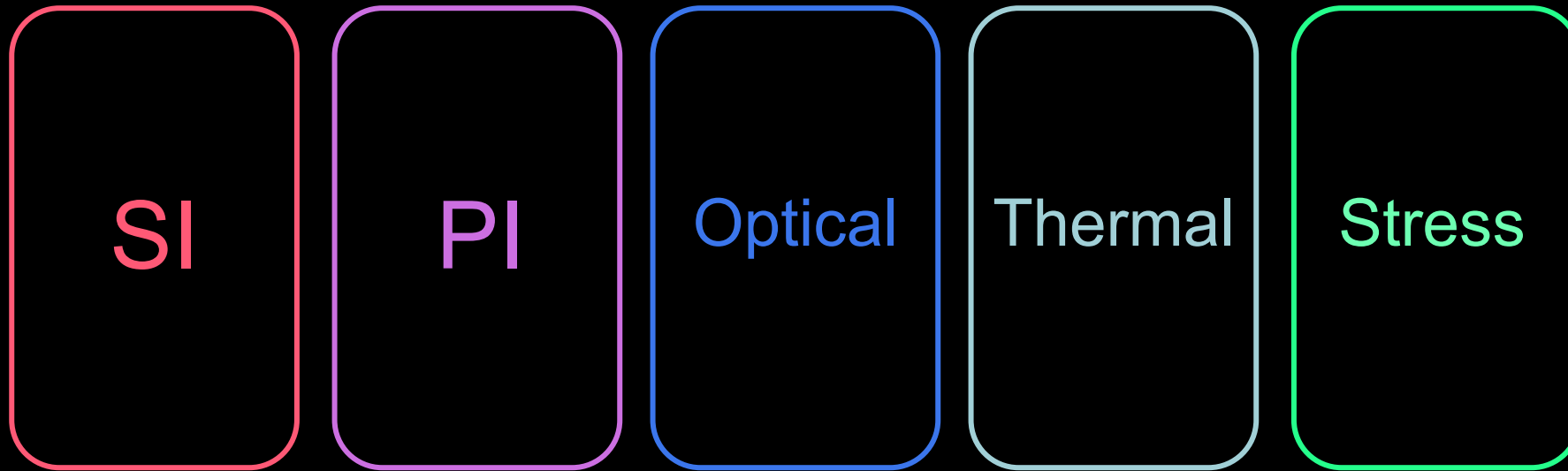
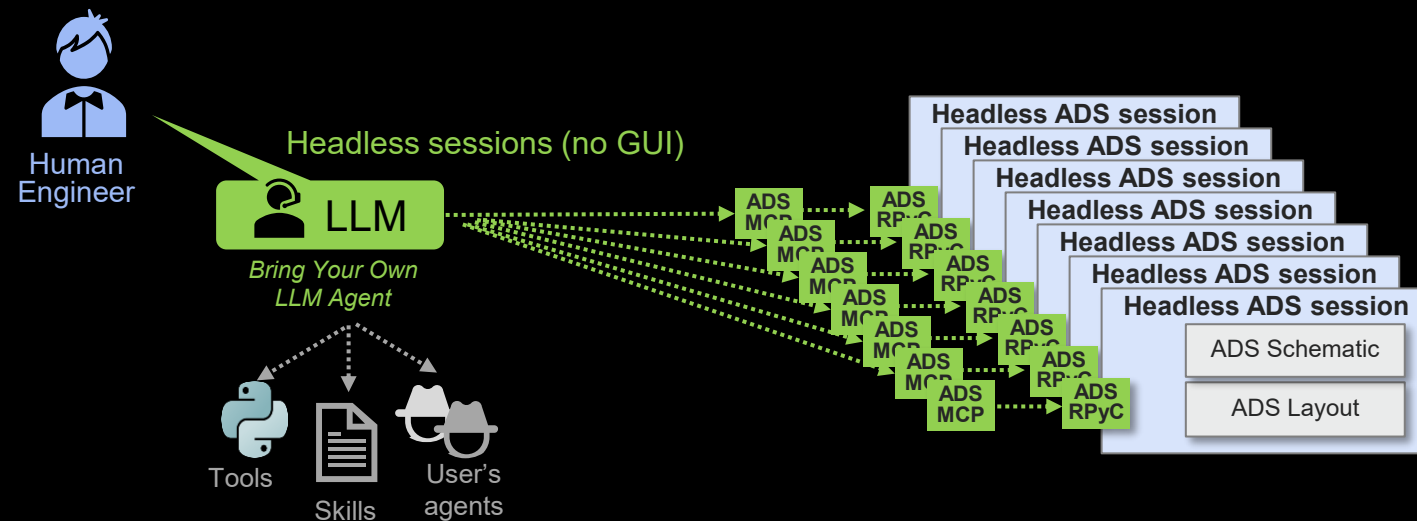
System level EOE design challenge

Ethernet interconnect standard - Cosimulation between VPI and ADS

Example for System Designer for Ethernet



Managing Complexity with Engineer-led Multi-Domain Exploration



Conclusion

- The Data center market is massive with significant levels of industry investment
- There are many engineering problems that are not yet solved
- Novel methods to manage thermal issues are actively being worked on
- Interconnects are moving away from copper to fiber or on-chip and on-package optics
- Workflows are fast evolving to be managed by LLMs

Thank you