



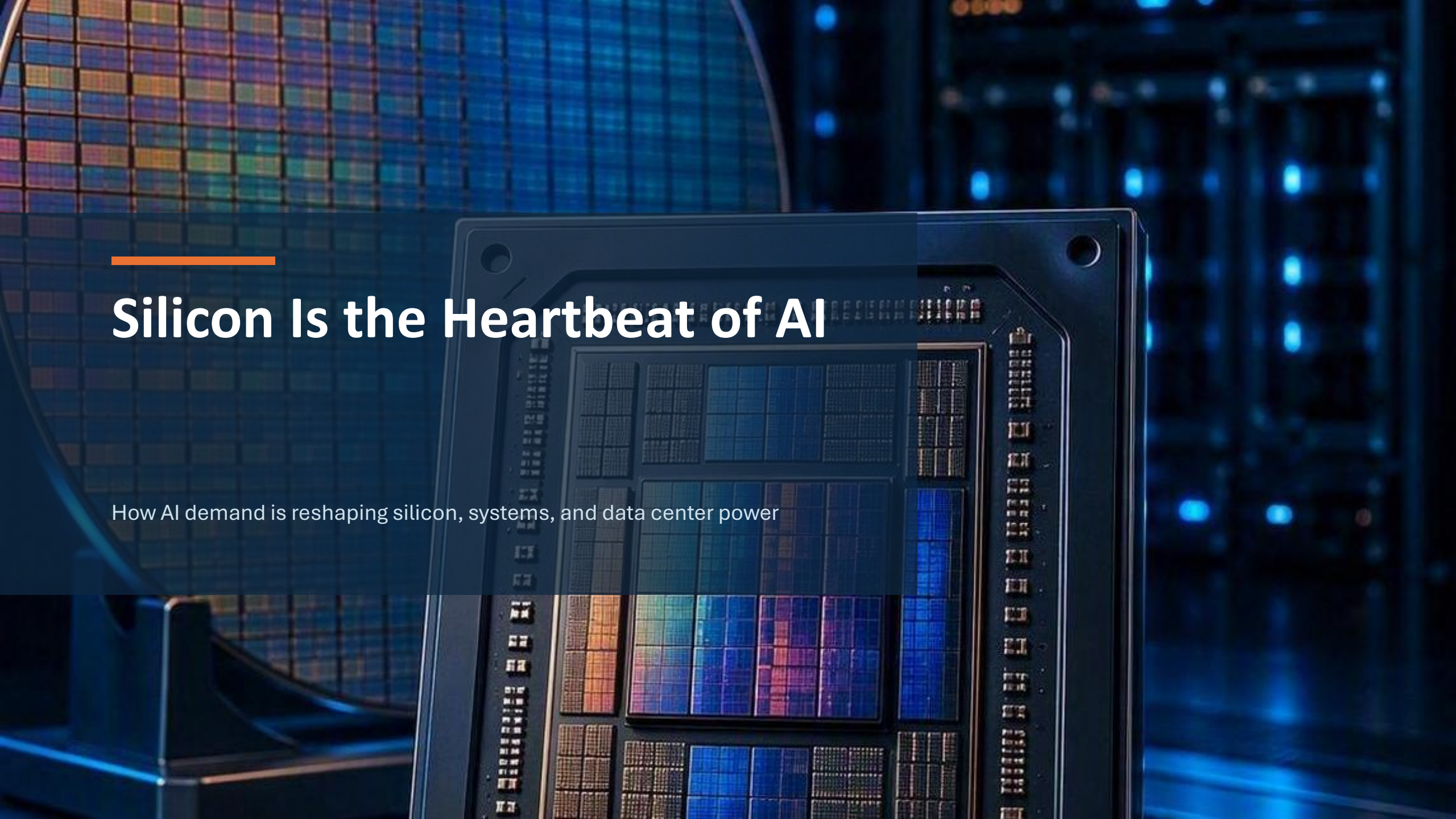
Considerations for Designing a Data Center for Large-Scale Semiconductor Design

Powering the Next Generation of AI Factories

Vik Malyala | Chief Business Officer, Supermicro

IEEE 2026





Silicon Is the Heartbeat of AI

How AI demand is reshaping silicon, systems, and data center power

From Semiconductor to Data Hall to AI Workloads

01

From Semiconductor → Data Center

Power, Package, Pin-out, Density, SerDes
CPU, GPU, Switch, DPU, PCIe switch silicon

02

Semiconductor → Motherboard

The board-level challenges Server vendors inherit

03

Motherboard → Server → Rack

Mechanical, Power, and thermal integration

04

Cluster → Data Center

Liquid Cooling - Techniques

05

AI Workloads → Semiconductor Design

CPU, GPU, switch, PLX, flash storage

06

Call to Action → Industry and Academia

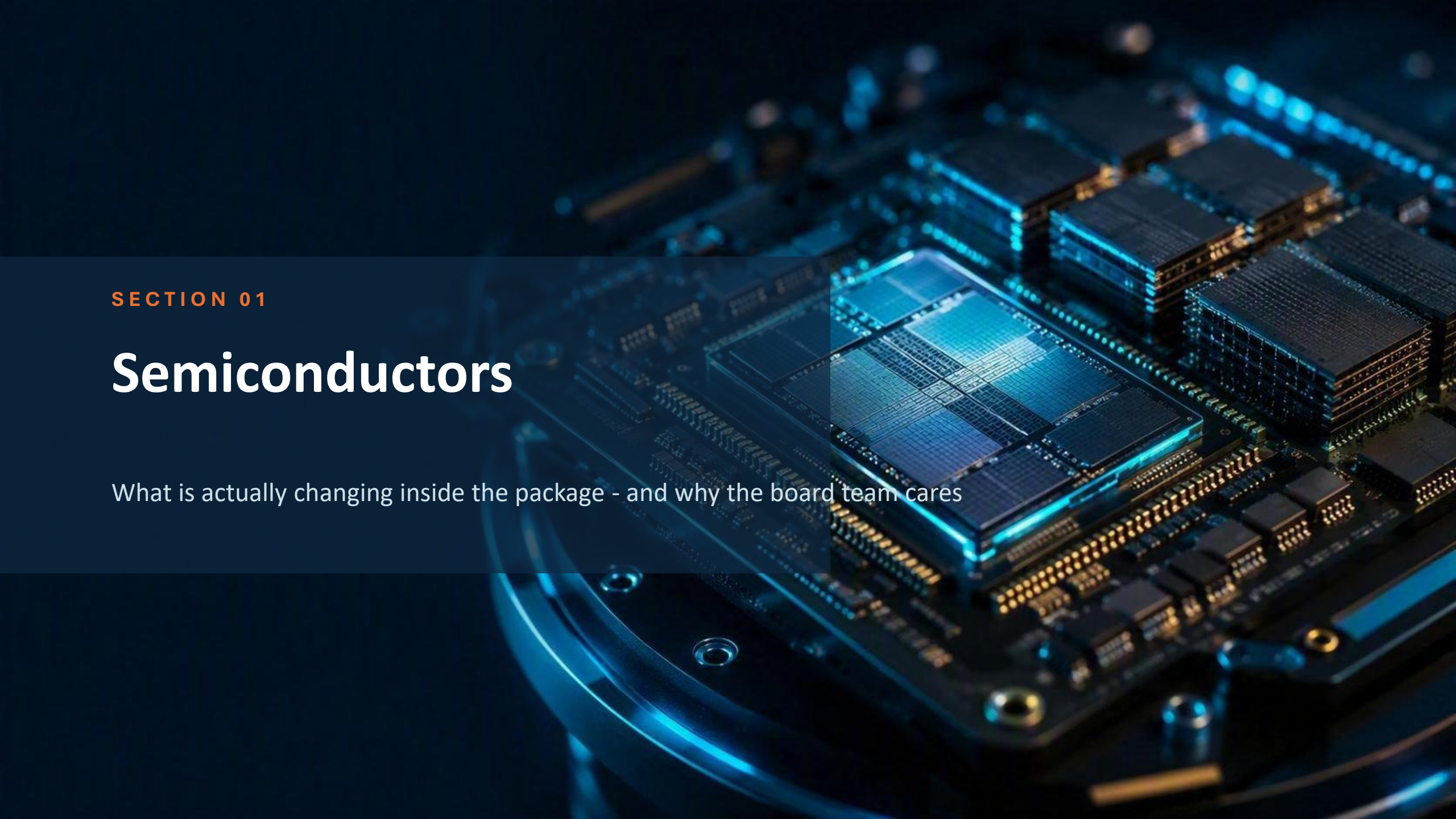
AI driving efficiency, optimization, cost and quality

From Semiconductor to Data Center

From a transistor to data center facility - each hop inherits the one before it



Compute density is no longer limited by lithography alone - it is limited by how many watts we can deliver to a Data Center per Square meter and number of Tokens we can generate per watt



SECTION 01

Semiconductors

What is actually changing inside the package - and why the board team cares

Transistors, Package, Pinout, Power and Weight

The socket assembly is now a structural problem, not a placement problem



Transistor

50+ Billion

- Advanced packaging
- Multi-die and 3D stacking
- Including HBM



Pin count

6,000-8,000

- Higher speed data transmission
- High count Power and Ground Pins
- Socket load runs to hundreds of pounds of force



Power

1000+ Watts

- High TDP Silicon with complex Voltage-Regulators



Board Design

- High count, pins, high wattage, bit rates, and larger packages together make board design challenging

SECTION 02

Semiconductor to Motherboard

Where die-level decisions become layer counts, materials and square inches

Key challenges in Motherboard Design

Power integrity

Multi-phase VRs. 48 V → 12 V → 0.7–1.0 V. Decoupling, PDN impedance, and sensing loops.

Signal integrity

PCIe 5/6, 112G SerDes, DDR5, 1.6G Networking. Loss, crosstalk, via stubs, back-drill, materials.

Mechanical

Socket force, BGA warpage, heat-sink /cold-plate clamp load, shock/vibe, connector wipe.

Thermal

CPU/GPU, VR MOSFETs, retimers, DIMMs, and optics add heat to Motherboard design.

Manufacturing

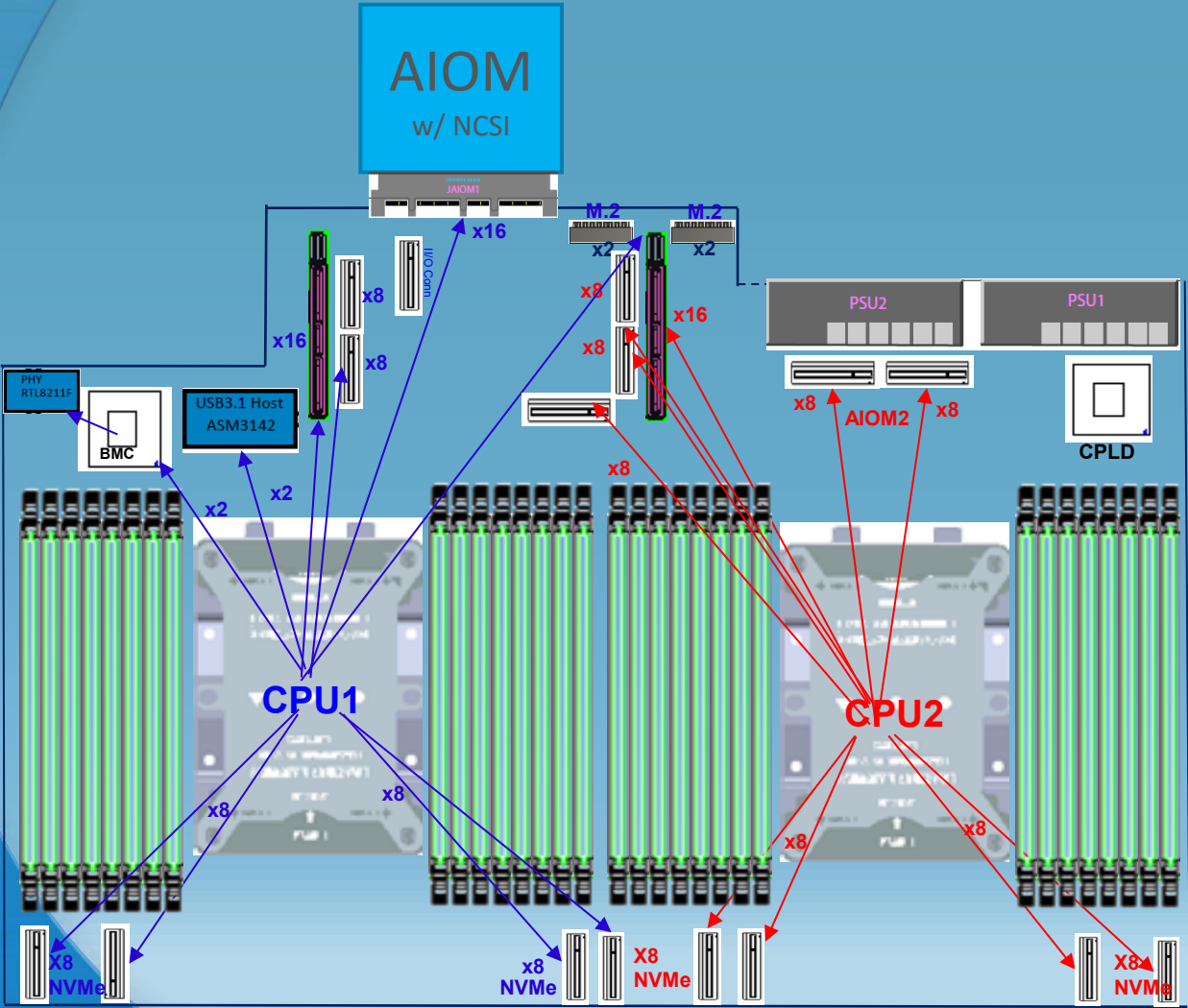
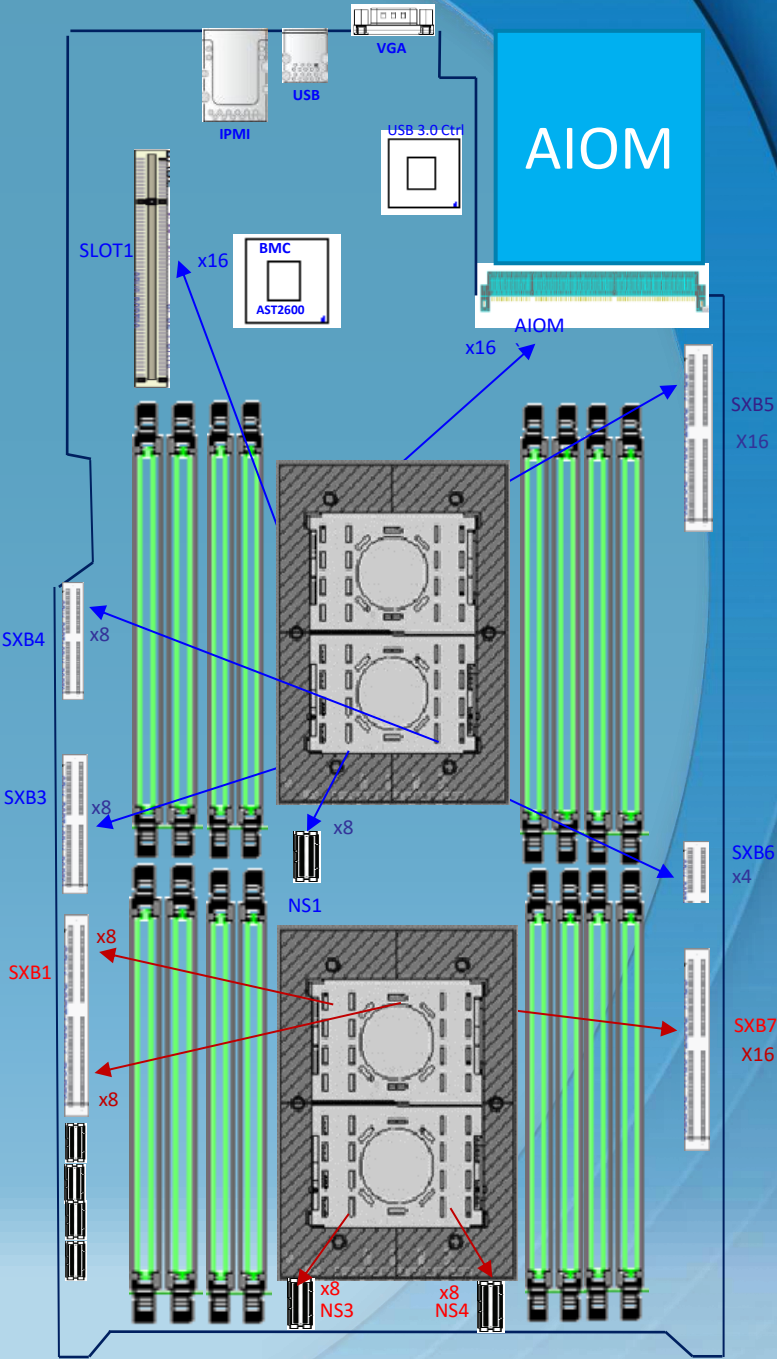
20–28+ layer boards, HDI, stacked microvias, yield, press-fit, and rework limits.

Compliance

SI/PI sign-off, EMC, NEBS/GR, safety spacing at high current, and liquid-loop leak detection.

Motherboard Design Techniques

Dual CPU and 8/16 Channel Memory Channel Designs



SECTION 03

Motherboard to Server

Turning a motherboard into a serviceable, coolable, shippable machine

From Motherboard to Server

what the chassis must absorb

01

Motherboard

Keep-outs, I/O,
power connectors

02

Chassis

Air ducts, Shrouds,
Fans, manifolds,
stiffening

03

Power

VRM/ PDB / bus-
bar / 48–54 V

04

Thermal/Air Flow

HS / cold plate /
leak kit

05

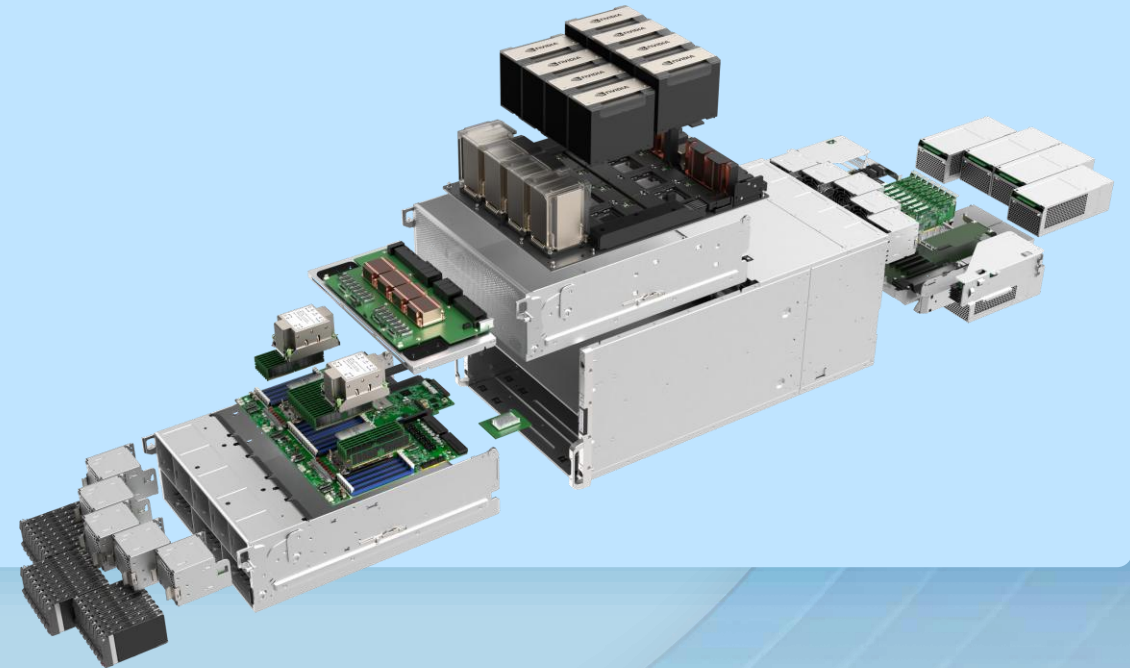
Cables

MCIO, SlimSAS,
M-XIO, Optics

06

Firmware

BIOS, BMC,
SPDM, Telemetry



SECTION 03

Server to Rack

Why power became the constraint, and what replaced the fan

CPU Compute



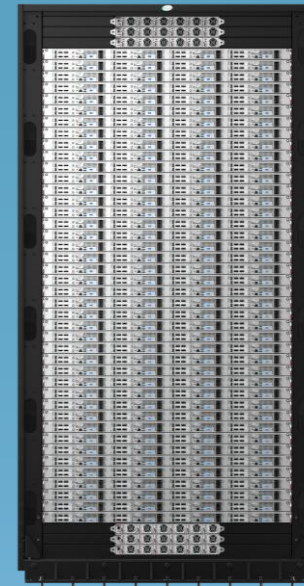
NVIDIA
Vera
Rack



AMD EPYC
FlexTwin
Rack

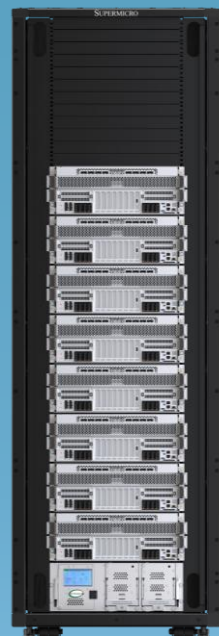


ARM AGI
Rack

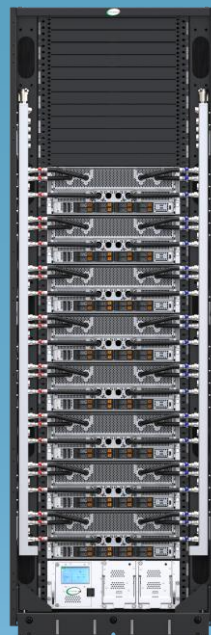


Intel
Xeon6
Rack

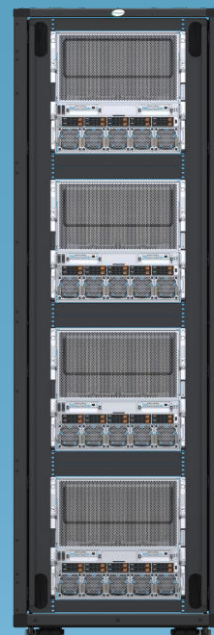
GPU Compute



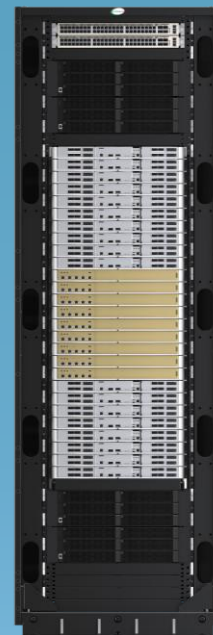
NVIDIA B300
Rack



AMD MI355
Rack



NVIDIA GB300
Rack



NVIDIA VR
NVL72



AMD Helios

Storage



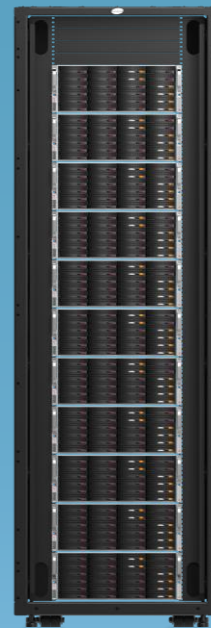
Petascale
Rack



CMX
Rack



Top Load 160 U.2
Rack



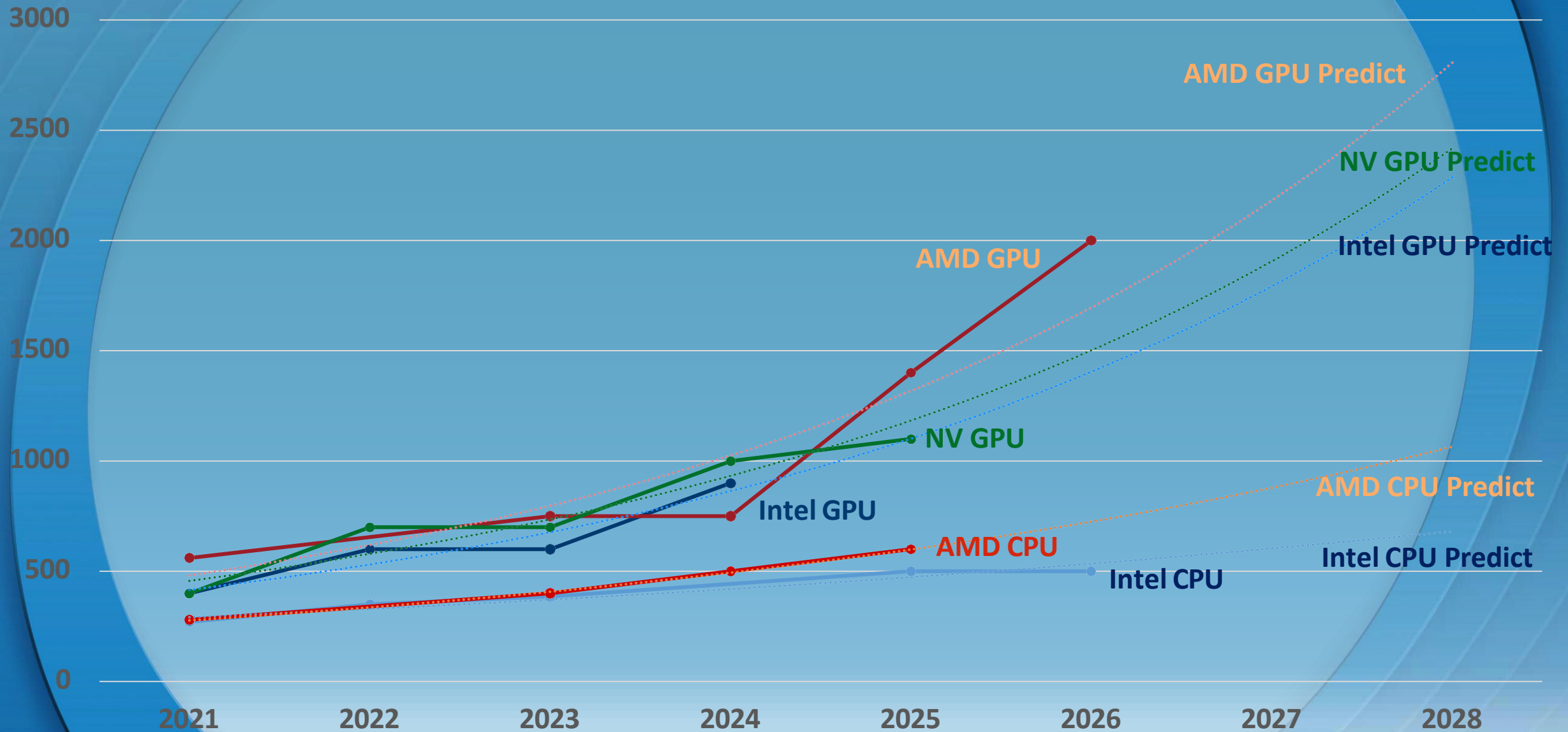
HDD
RACK

SECTION 04

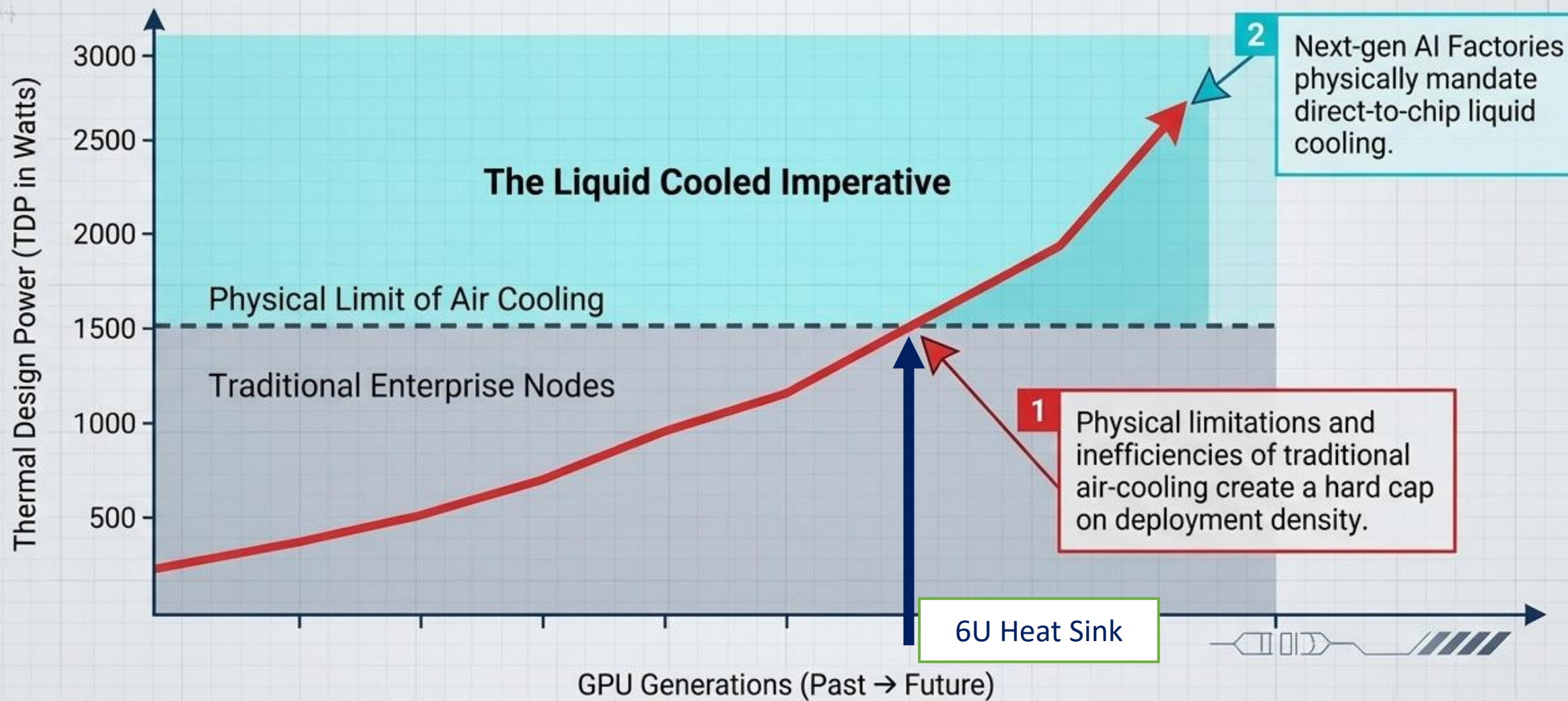
Air to Liquid

Why power became the constraint, and what replaced the fan

Silicon Thermal Design Power Trends



Breaking the Air-Cooling Limit



Why power became the constraint

Air ran out of heat capacity before silicon ran out of transistors



Rack density then 5-15 kW

- A decade of designs assumed this range
- Raised floor and CRAC units sized around it
- Most existing halls were built to this number



Rack density now 60-130+ kW

- A single AI rack can exceed a legacy row
- Dense racks are shipping at over 100 kW today
- Roadmaps point higher still



Where air stops ~30-40 kW

- Beyond this, airflow volume becomes impractical
- Fan power grows sharply and eats the power budget
- Acoustic and recirculation problems compound



Why liquid wins ~30x

- Water carries far more heat per unit volume than air
- Enables warm-water cooling and free cooling hours
- Reclaimed heat becomes a usable output, not waste

Air cooled to liquid cooled - the three paths

Retrofit, mainstream, and the one everyone asks about



Rear door heat exchanger up to ~80 kW

- Bolts onto an existing rack; servers stay air cooled
- The fastest retrofit path for an existing hall
- Needs facility water to the rack but not into the server
- Limited headroom as densities keep climbing



Direct-to-chip liquid (DLC) 70-98% heat captured

- Cold plates on accelerators, CPUs and increasingly memory
- Where new high-density builds have converged
- Residual heat still needs an air or rear-door path
- Leak detection, quick-disconnects and fluid chemistry to manage



Immersion cooling near 100%

- Entire server submerged in dielectric fluid
- Excellent thermal performance, no server fans at all
- Heavy tanks, fluid handling and messy servicing
- Component and warranty compatibility still a barrier

Server to rack design

Rack design is now a power-and-fluid product



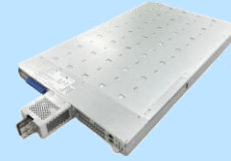
Rack form factor

- OCP ORv3, EIA 19", 21" deep AI racks. Height 42–52U. Depth grows for manifolds and bus bars.



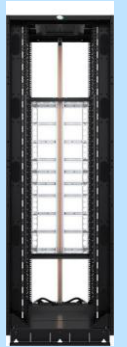
Power shelves

- 48–54 V DC shelves. Multiple kW per shelf. Hot-swap, paralleled.



Busbars

- Vertical DC busbar replaces dozens of power cords



Power whips

- High-amperage feeds from the floor PDU to the rack
- Connector class and phase balance planned per row
- Often the long-lead item in a deployment.
- Facility 3-phase to PDU/shelf



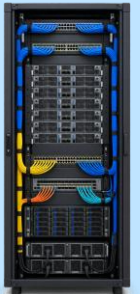
CDU/Side Car / Manifolds

- In-rack or in-row CDU when facility water is not at the aisle.
- Vertical supply and return distributing to every tray
- Quick-disconnects rated for hot service
- Needs planned access space and drip management



Cable management

- Hundreds of high-speed links per rack
- Bend radius and weight support designed in
- Serviceability is decided here, in practice



SECTION 04

Data Halls and Data Centers

Why power became the constraint, and what replaced the fan

Rack to cluster to data center

The unit of deployment is now the cluster, not the server



Rack

- The smallest complete power and cooling unit
- Commissioned as a tested assembly, not built in place



Cluster

- Racks wired as one scale-out fabric
- Fabric topology fixes the physical row layout
- Scheduled and operated as a single machine



CDUs and sidecars

- Isolate the facility loop from the technology loop
- In-row and in-rack options trade capacity for footprint
- Filtration and fluid chemistry monitored continuously



Chillers and towers

- Warm-water operation unlocks free-cooling hours
- Dry coolers cut water use at an efficiency cost
- Climate and water availability drive site selection



Electrical plant

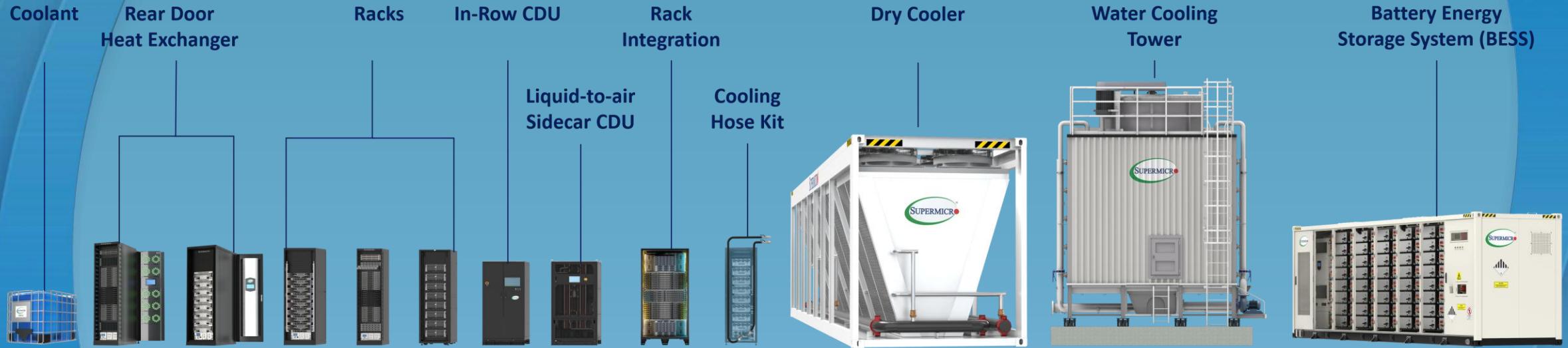
- Generators, switchgear and UPS sized to the block
- AI load steps are fast and can stress the plant
- Grid interconnect is often the true schedule driver



Commissioning

- Fluid loops flushed and proven before IT load
- Fabric validated before the first training job
- Facility lead time exceeds IT lead time, routinely

Data Center Building Block Solutions™ (DCBBS)





SECTION 05

AI Workloads Transforming Semiconductors

How Generative and Agentic AI transforming Semiconductor Industry

AI Workloads – Training vs Inference

AI demand is a systems problem, not only a chip problem

Training clusters

Tens of thousands of GPUs, all-to-all fabrics, multi-MW halls. Job completion time is gated by the weakest link: silicon, Motherboard, NIC, switch, or cooling.

Inference factories

Continuous high utilization, power-constrained sites, density over peak FLOPS. TCO is watts, tokens, and availability.

The coupling

Every extra 100 W at the package becomes bus-bar current, CDU flow, chiller tons, and generator sizing. Silicon roadmaps now write facility roadmaps.

AI Workloads From Healthcare to EDA

From a transistor to data center facility - each hop inherits the one before it

01

Finance and Banking

Algorithmic Trading
Fraud Detection
Risk Management

02

Healthcare and Life Science

Medical Imaging
Diagnostics
Genomics
Drug Discovery

03

Robotics and Autonomous Systems

Industrial Automation
Autonomous Vehicles
Drones

04

Retail and Commerce

Inventory
Forecasting
Dynamic
Recommendations

05

Logistics Shipping and Receiving

CDUs, rows,
containment

06

Semiconductors

IC Design
EDA Tools
Wafer Manufacturing
Bin and Sort

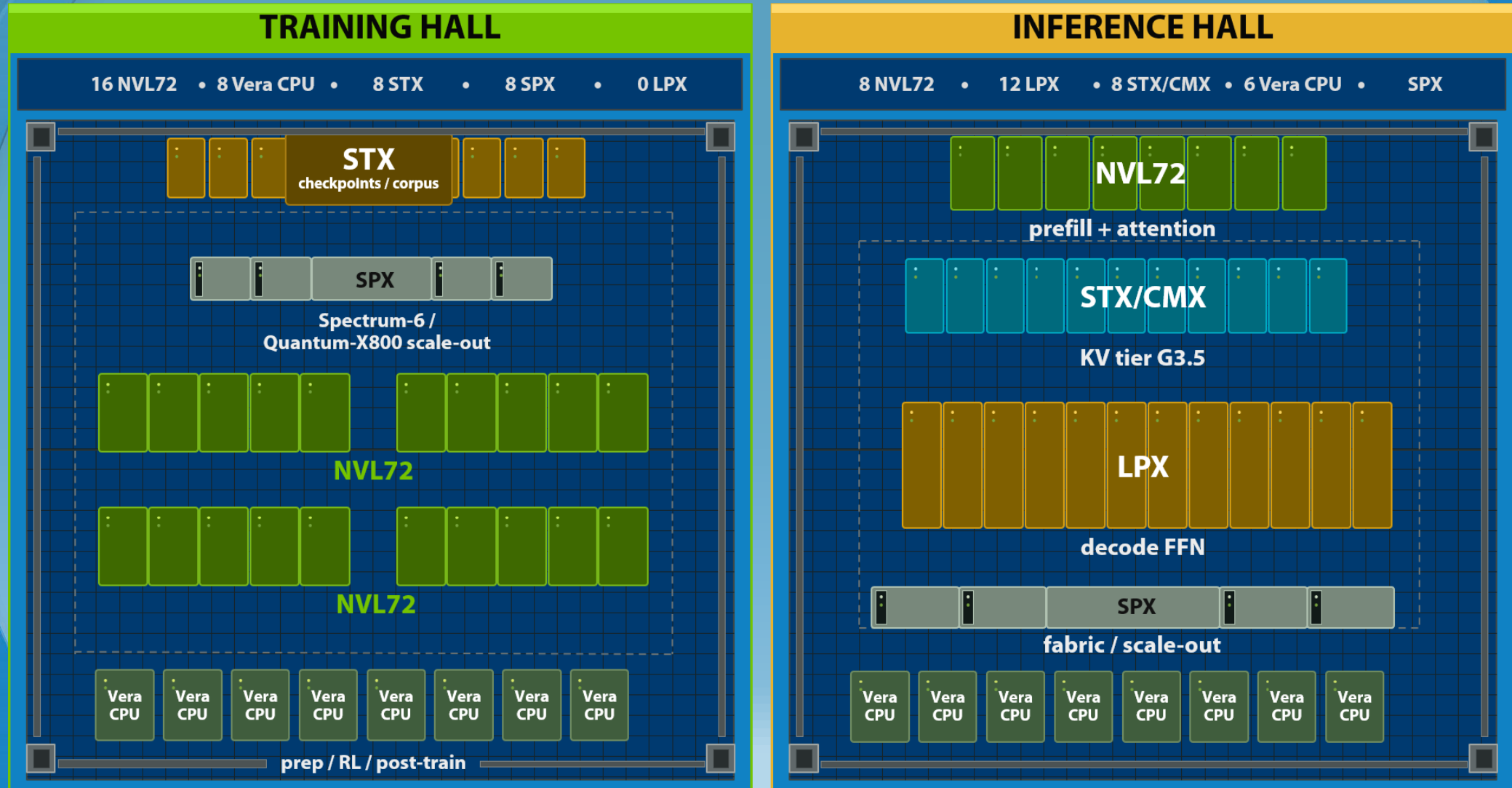
AI Workloads From Semiconductors

Compute Farms - Each workload demands different – Core Count, Clock Frequency, Memory Capacity, Storage and Networking



Vera Rubin POD Floorplan – Training Hall vs Inference Hall

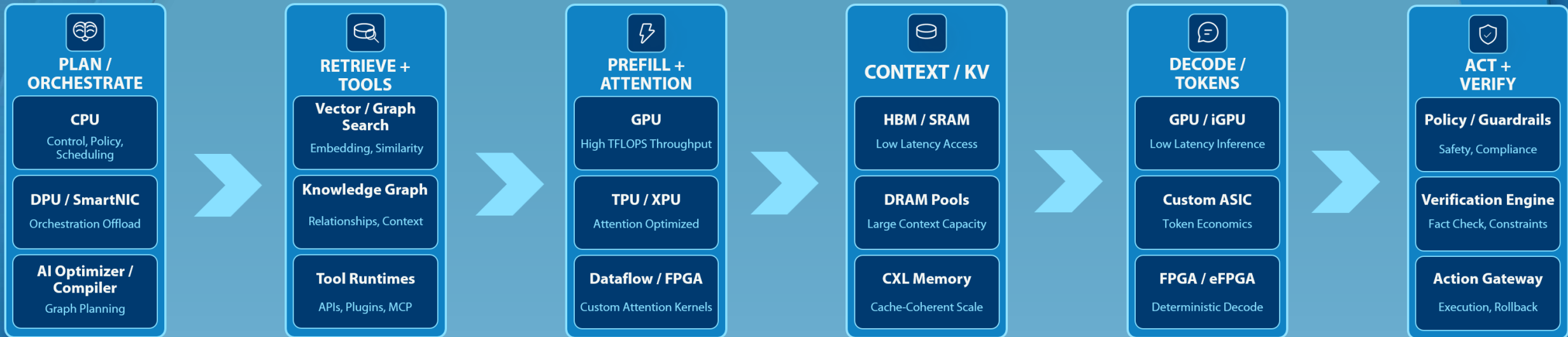
40-rack POD building block · 16× NVL72 = 1,152 Rubin GPUs · companion rack mix is planning, not an SKU BOM



Heterogeneous Agentic AI Factory

Pick per stage, not per vendor

Same workflow, swappable silicon, air-cooled PCIe to liquid rack-scale.



FABRIC & INTERCONNECT



NVLink / NVSwitch



CXL / PCIe Gen5/6



RDMA / RoCE



IP over Fabric Telemetry & QoS

Low-latency • High-bandwidth
Rack-scale • observable



SOFTWARE GLUE



OPEN STANDARDS
APIs, Protocols, Schemas



AGENT ORCHESTRATION
Workflow, State, Memory



OBSERVABILITY
Metrics, Traces, Logs



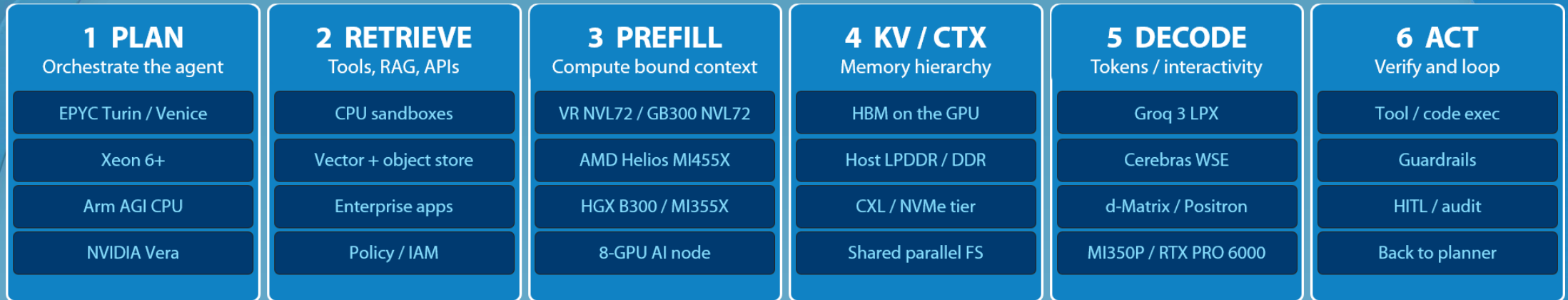
SECURITY & GOVERNANCE
RBAC, Secrets, Audit



PORTABILITY LAYER
Abstraction, Adapters, Contracts

Heterogeneous Agentic AI – Pick Per Stage, Not Per Vendor

Same workflow, swappable silicon: choose the best engine at every stage of the pipeline



DEPLOY WHERE THE WORKLOAD FITS — three halls, one control plane

HALL A • LIQUID RACK-SCALE

Frontier train + long-context prefill

VR NVL72 · GB300 NVL72 · AMD Helios
(2× MI455X)

NVLink 6 or Infinity Fabric inside the rack. 190–230 kW
class. Direct-to-chip liquid.

HALL B • NODE / HGX

Departmental train + high-concurrency infer

HGX B300 · MI355X & OAM · 8-GPU air or
hybrid nodes

Standard 19" or OCP. Mix vendors by row. Ethernet or IB
scale out.

HALL C • ENTERPRISE PCIE

Branch / sovereign / air-cooled estate

RTX PRO 6000 · MI350P · d-Matrix / Positron cards

Drop into existing racks. No NVL72. Fast enough for most
enterprise agents.

FABRIC Scale-up stays inside a vendor domain (NVLink · Infinity Fabric). Scale-out is shared IB Quantum · Spectrum-X · Ethernet/RoCE default for enterprise.

GLUE Dynamo / vLLM / SGLang / TensorRT-LLM / ROCm / MIG. K8s-aware router across pools. Do not pin every agent step to one POD SKU.

The Data Advantage: Turning Enterprise Data into Intelligence

LLM, generative and agentic AI turn proprietary silicon data into better chips at every phase



Architecture / ISA

YOUR DATA

PPA models, workload traces, telemetry from shipped parts

AI ADVANTAGE

LLM agents explore trade-offs against your real workloads, not generic benchmarks



Design / RTL

YOUR DATA

Decades of RTL, design reviews, bug databases, proven IP

AI ADVANTAGE

Assistants generate and review RTL in your house style and reuse silicon-proven IP



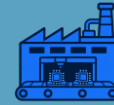
Process

YOUR DATA

PDK history, corner data and yield per node

AI ADVANTAGE

Models flag timing and power closure risk early and steer floorplan and cell choices



Production

YOUR DATA

Yield, bin splits, process drift, fab excursions

AI ADVANTAGE

Agents correlate yield loss to design constructs and feed fixes into the next stepping



Verification

YOUR DATA

Regression results, coverage databases, bug and escape history, ATPG patterns and fail logs

AI ADVANTAGE

Targets regressions at high-risk logic, closes coverage faster, and learns from past escapes to cut test patterns



Quality

YOUR DATA

Failure analysis reports, ELF and burn-in results, field returns, RMA and reliability history

AI ADVANTAGE

Clusters failure signatures to find root cause faster and predicts which design constructs drive early-life failures

Tools are available to everyone - the proprietary data behind them is not. Business advantage comes from your own silicon history.



SECTION 06

Call to Action

Where we go from here with AI tools

The gap: challenges and the EDA tooling to close it

MEDIUM TO LONG TERM

Challenge in data center chip and system design	What the EDA tooling must deliver
Power and thermal now constrain design as much as timing	Power- and thermal-aware co-design across die, package, board, and rack — not a post-layout check
Chiplets and advanced packaging multiply the design space	Multi-die planning, cross-die timing and thermal closure, and standardized interconnect models
AI accelerators are co-designed with the workload	Workload-driven architectural exploration with credible, fast performance-per-watt models
Verification cost grows faster than design size	ML-assisted coverage closure and test selection, with reproducibility and auditability
Flows assume dedicated farms, not shared AI floors	Schedulers and tools that are telemetry-aware and cooperate across heterogeneous resources

A call to action for industry and academia

WHERE WE GO FROM HERE

Industry

- Publish workload-representative benchmarks for mixed EDA and AI floors
- Standardize telemetry schemas across facility, hardware, and scheduler
- Design servers and cooling as one system, with the roadmap density in mind

Academia

- Open models for power, thermal, and performance at rack and floor scale
- Research on ML-in-the-loop verification that is reproducible and auditable
- Curricula that treat the data center as part of the chip design problem

Accelerate Everything

The next generation of chips will be designed in data centers that were themselves designed for them.

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