
SYNOPSYS®
Our Technology, Your Innovation™

Emerging Technologies for Computing Paradigm Shift

Brandon Wang
VP, Corporate Technology Strategy

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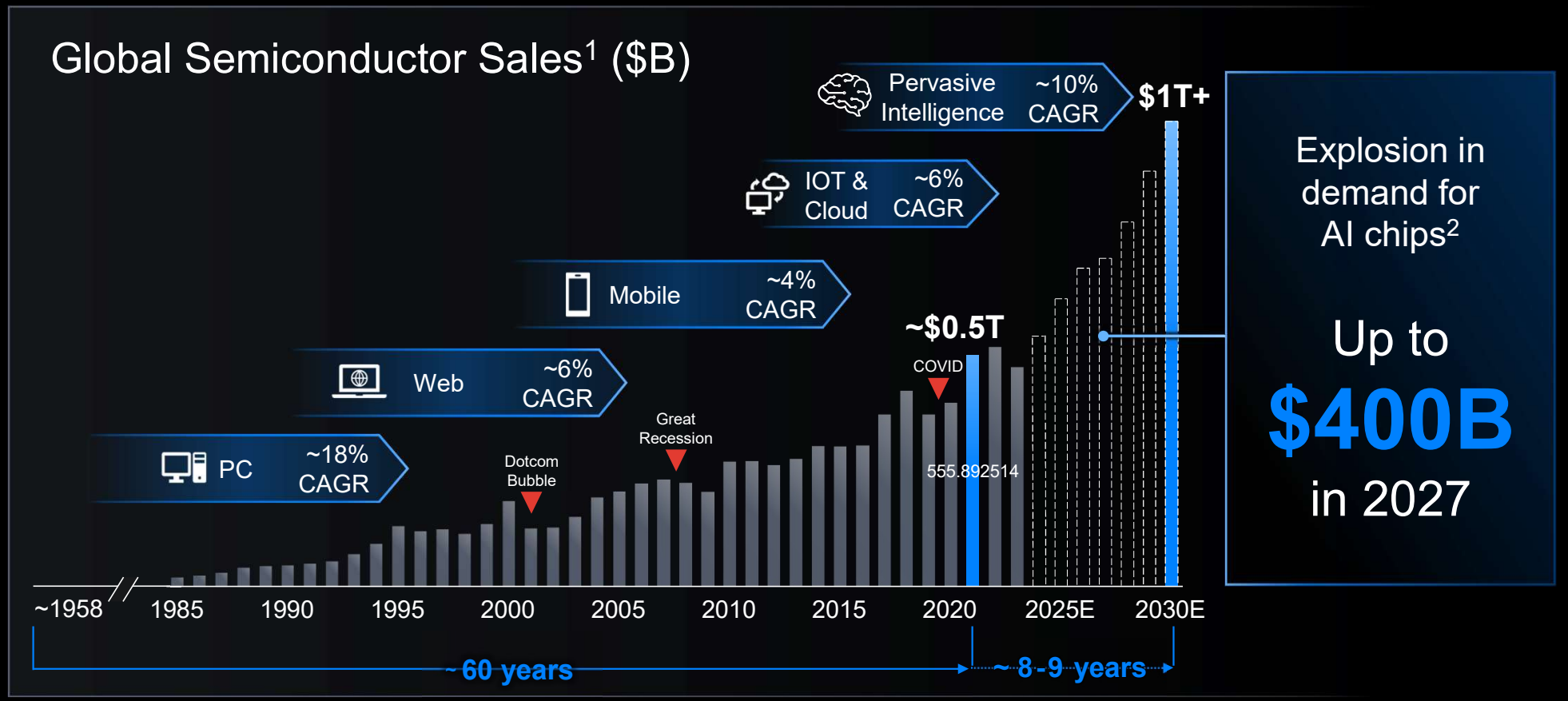
Sharp Acceleration in Semiconductor Demand



1. Sources: SIA/WSTS (historicals); forecasts based on Gartner, TechInsights, IBS, SIA/WSTS and consensus analyst forecasts for leading semiconductor companies
2. Sources: Gartner, AMD, Nvidia, Intel, Goldman Sachs

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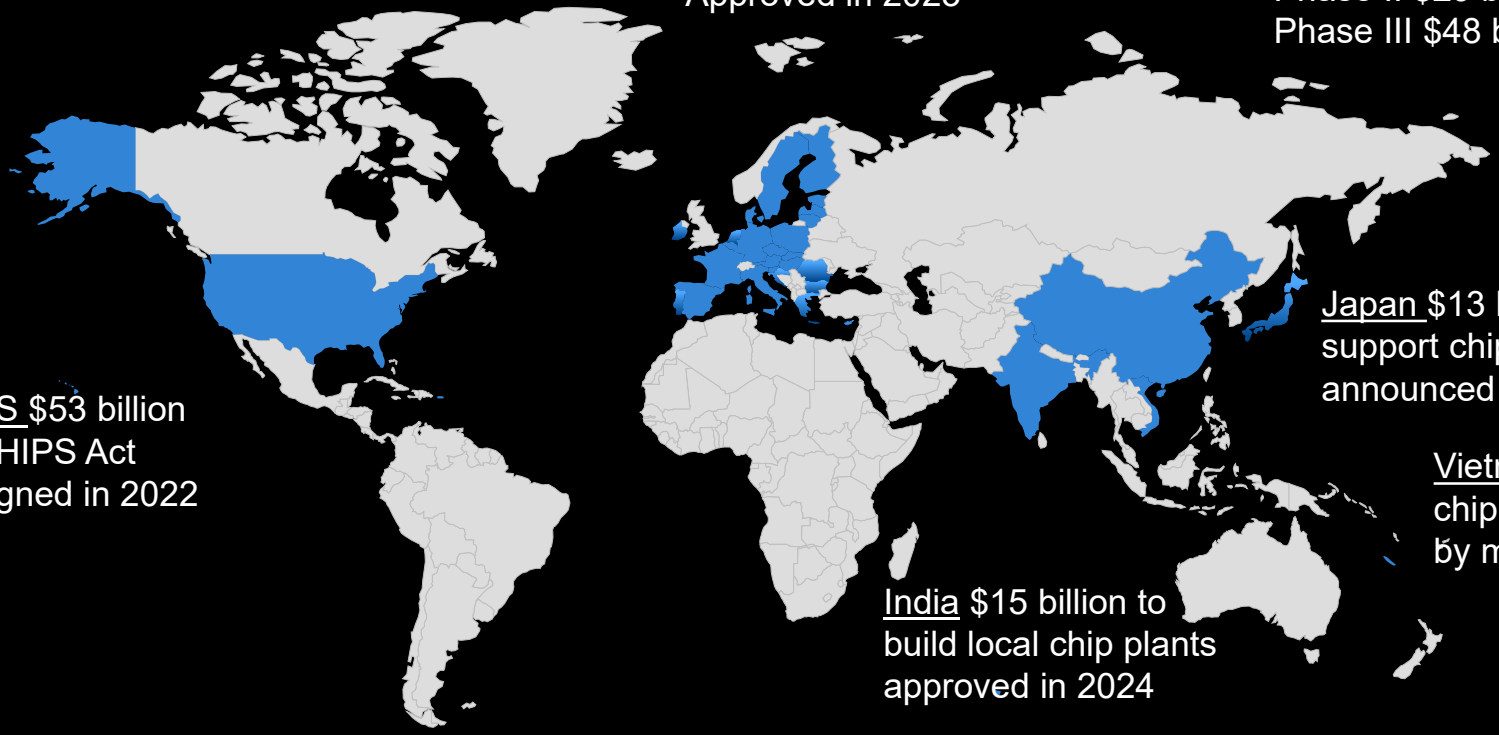
Great Time for Chip Industry



EU $47 billion
European Chips Act
Approved in 2023

China Big Fund
Phase I $22 billion 2014
Phase II $29 billion 2019
Phase III $48 billion 2024

Japan $13 billion to
support chip industry
announced in 2023

Vietnam to roll out
chip incentive policy
by mid-2024

US $53 billion
CHIPS Act
signed in 2022

India $15 billion to
build local chip plants
approved in 2024

VC-backed Chip Startups Closed 175 Deals, Raised $5.3 Billion in 2024 1H

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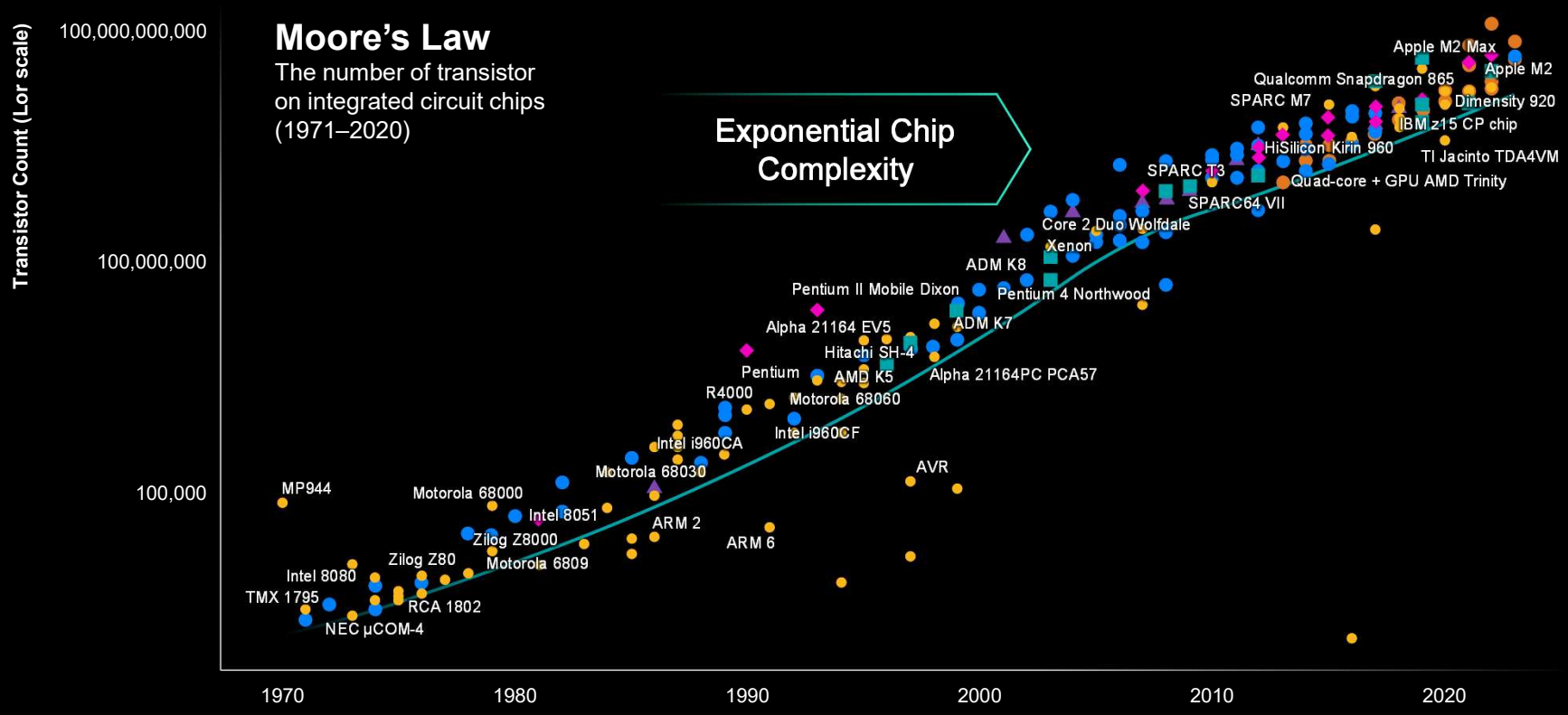
Transistors are NOT getting more efficient, Pushing the Limits of Chip Design



Source: Wikipedia – Transistor Count: https://interludeone.com/posts/2021-04-21-chips/chips_files/figure-html/unnamed-chunk-4-1.png

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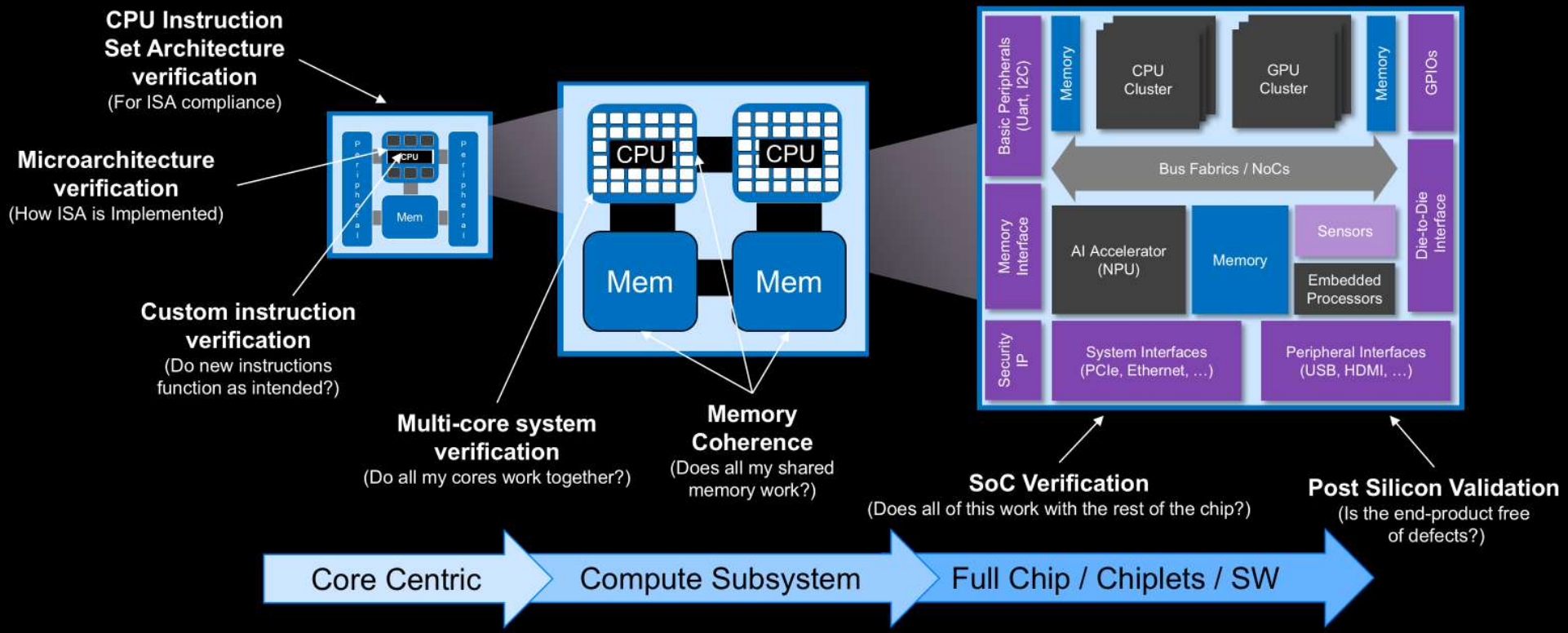
Customer Problem Scope Is Rapidly Getting Complex

From ISA through CPU, arrays of CPUs and Systems on Chips / of Chiplets



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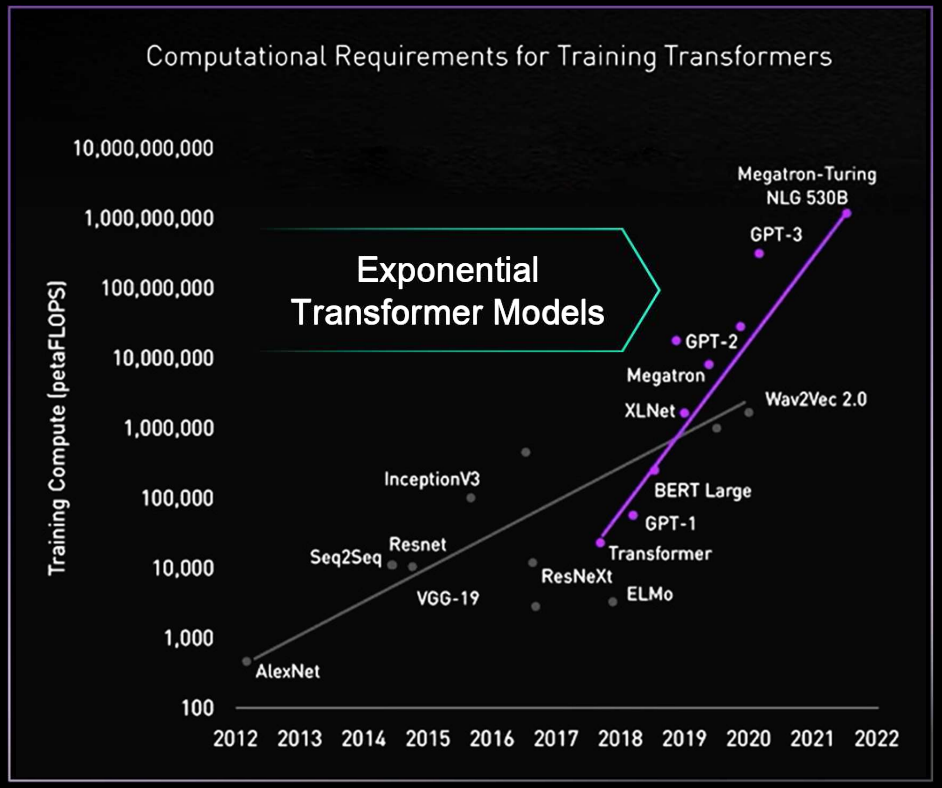
Newer Models Further Pushing Limits of Compute



All Models Excluding Transformers:

8X / 2 years

Transformer AI Models:

275X / 2 years

Context-Aware Transformer Models Come at a Price

Source: https://blogs.nvidia.com/blog/2022/03/25/what-is-a-transformer-model/

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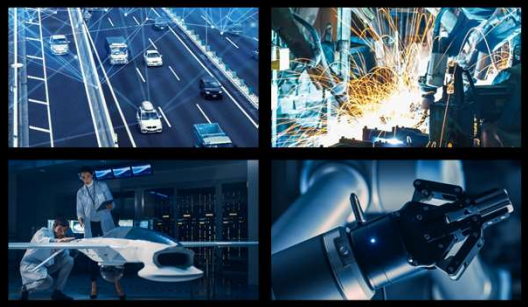
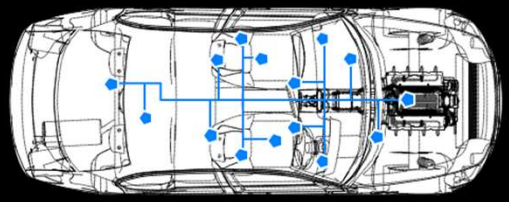
Increasing Silicon and Software Content In Systems Products



Autonomy and software-defined systems reshaping industries



Systems companies re-architecting products, business models and development processes

Driving demand for massive compute, both at the edge and the data center

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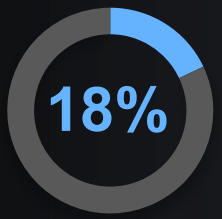
Systems R&D Processes Are More Complex, More Costly

YESTERDAY

TODAY

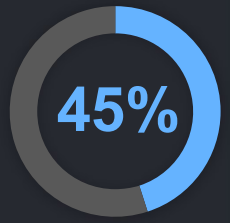
% of electronics in the cost of a new car[1]…



2000

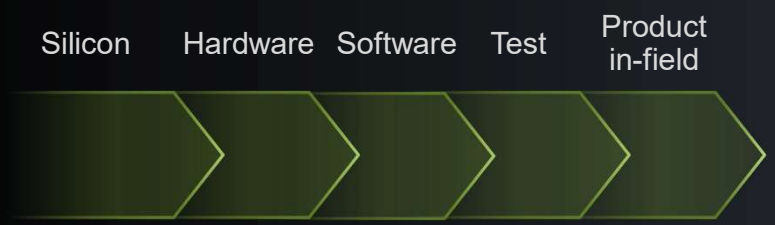
Increasing cost of electronics

…increasing by ~2.5x



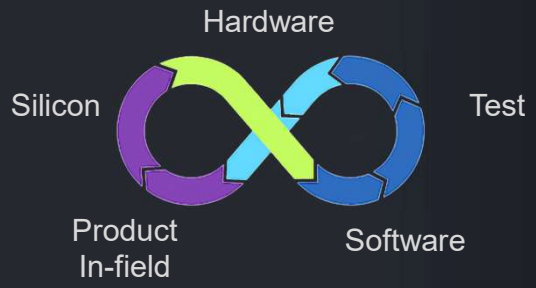
2030

Sequential design flows…



New design flows

…are now continuous



Source: "Semiconductors – the Next Wave", April 2019, Deloitte Report

1. Cost contribution of automotive electronics and semiconductor content per car

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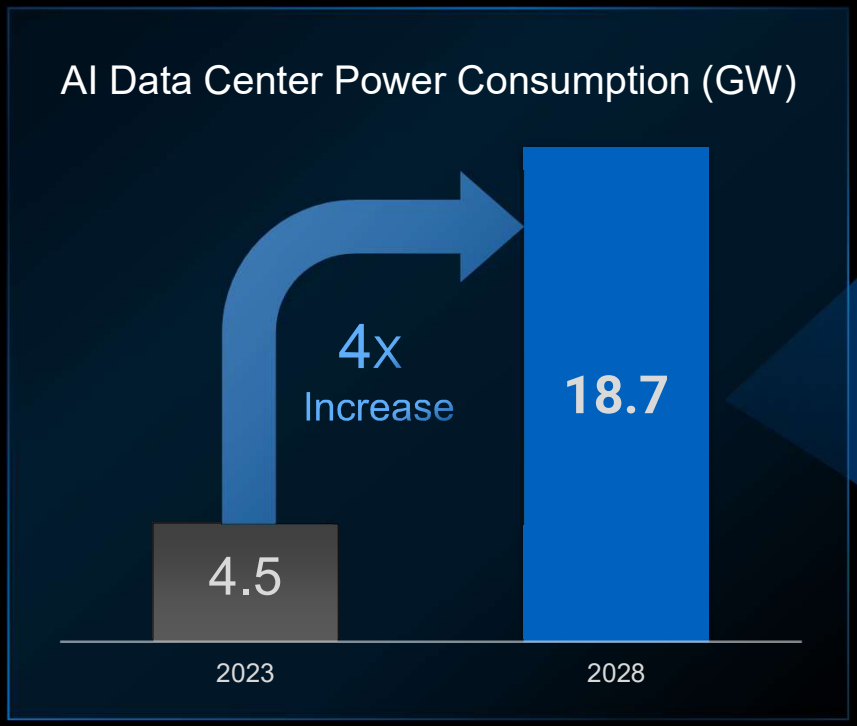
AI Driving Unprecedented Power Consumption



Source: Schneider Electric, December 2023

nVIDIA H100 GPU

700 Watts*

Source: Schneider Electric, December 2023 ** Thermal Design Power*

ChatGPT request vs Google search

25x More Power

Source: RISE Research Institutes of Sweden, Oct 2023

AI Energy Consumption by 2030

2x France

Source: The Brussels Times Newsroom May 2024

Software to Device Solution Needed to Address the Magnitude of Power Consumption

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Huge Amount of Water Usage is Also UNSUSTAINABLE

Current Cooling Solutions room-temperature liquid colling

- HPC environments moving from hybrid air-liquid cooling to just liquid cooling @ higher flow rates
- This solution will not be enough to maintain system temperature and functionality
- Due to expensive packaging for high power dissipation capabilities

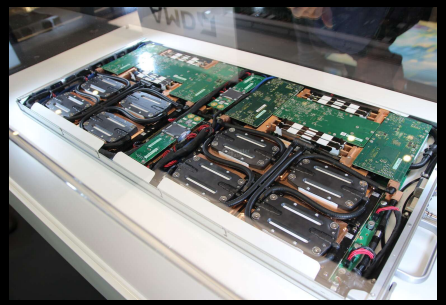
Google's Global Data Center in 2021 Water Usage

4.3 Billion Gallons

Source: Google, 2022

Frontier (#1 most powerful supercomputer) liquid-cooled

~6,000 gallons per minute



Source: Bloomberg, 2023

Innovative Cooling Solutions Needed to Address the Unsustainability of Water Usage

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The era of

PERVASIVE INTELLIGENCE

Artificial Intelligence

Exponential productivity and efficiency gains

Silicon Proliferation

More silicon content everywhere

Software-Defined Systems

New applications, new methodologies

Silicon to Systems Design Solutions

New design paradigm; Solving Energy challenges while addressing complexity

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Emerging Technologies
Addressing the Challenges in the Era of Pervasive Intelligence

Silicon Complexity

The need for custom silicon and the growing complexity of chip design

Silicon & Systems Intersection

Growing at the intersection of hardware and software

Compute & Energy Limits

Enhance compute power and be sustainable

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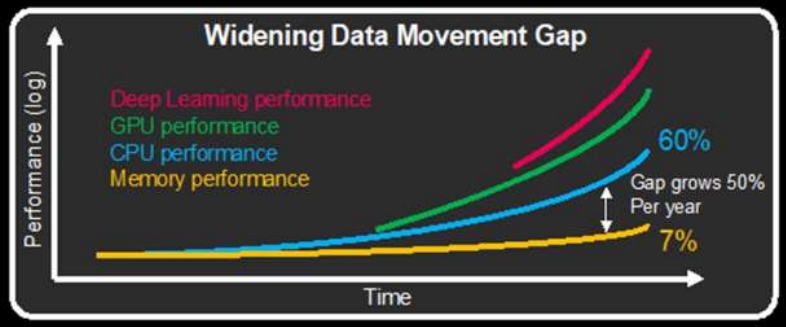
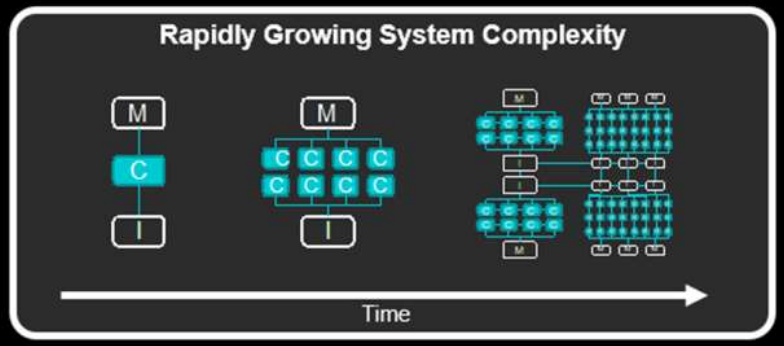
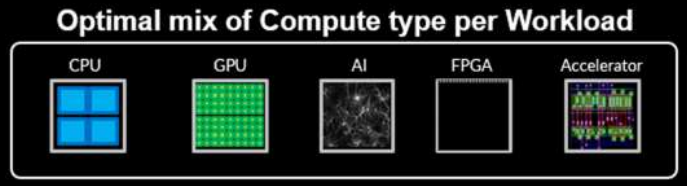
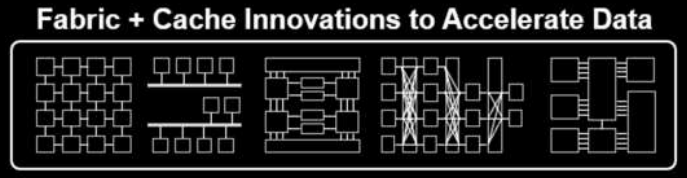
Silicon Complexity

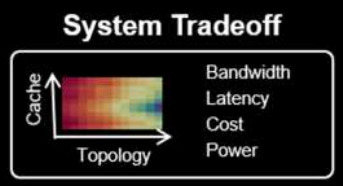
Customers Adopting New Design Paradigms in Computing

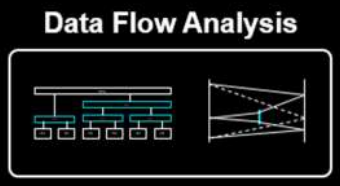






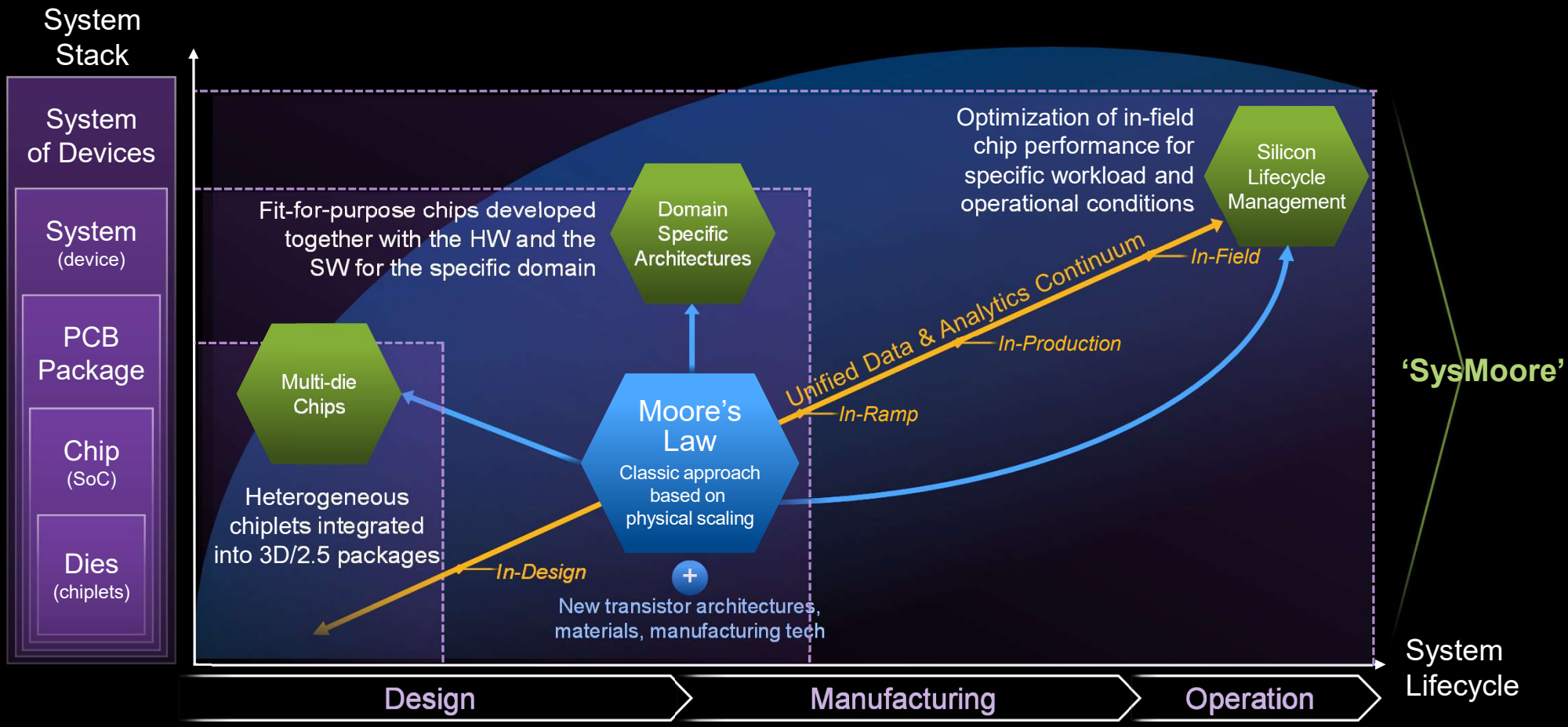






Source: Baya Systems, 2024

Meeting Explosive Compute Demand Requires New Paradigm



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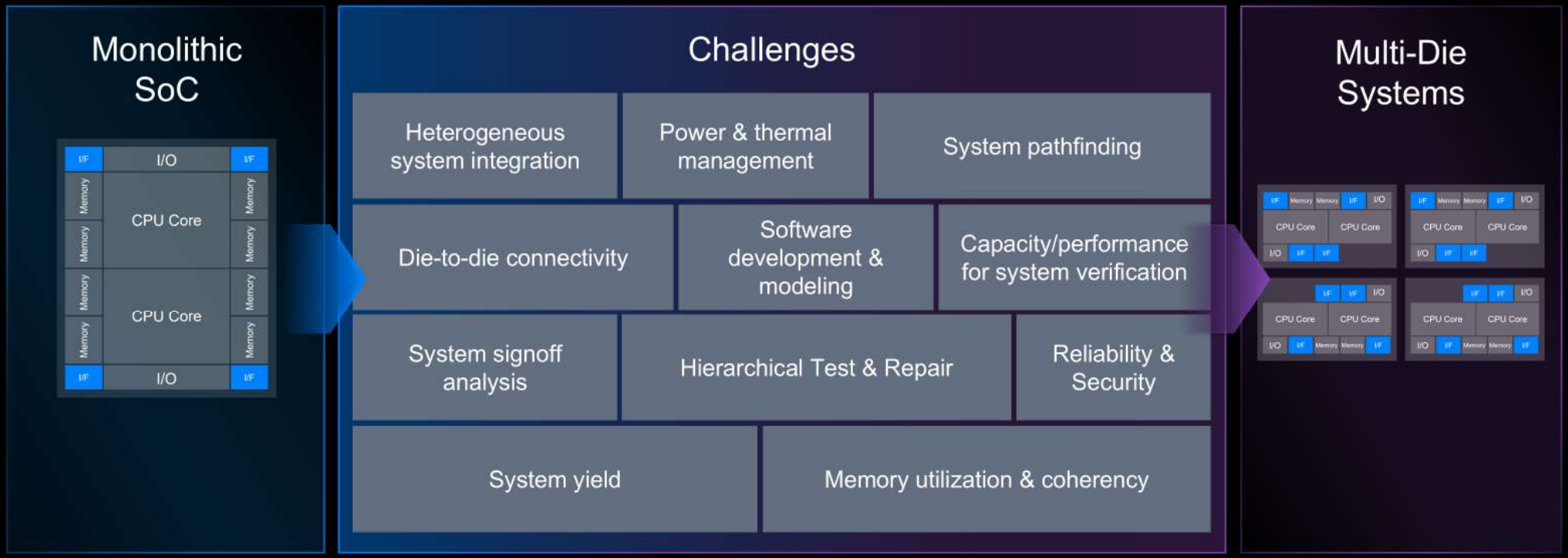
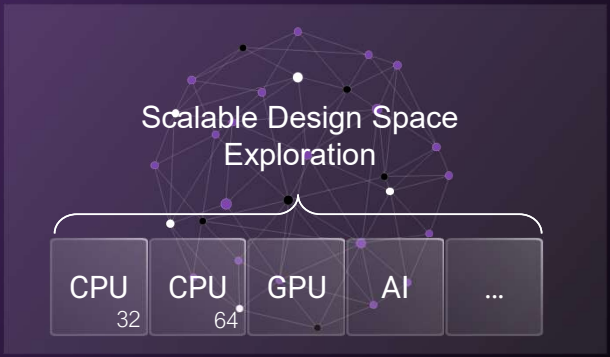
Heterogeneous Systems Design Challenges



Early Architecture Exploration For Multi-Die Systems

Partitioning & Optimization to Accelerate Architecture Realization with Platform Architect

PARTITION INTO DIES/CHIPLETS

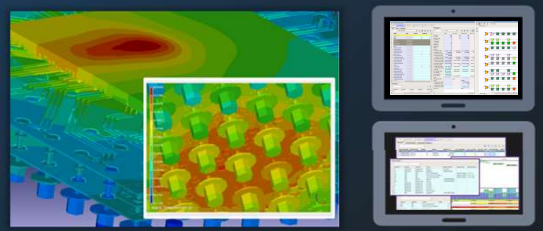


Separate system into its functions, scale functions across multiple dies

Meet scaling, fabrication, and functionality requirements

OPTIMIZE MULTI-DIE SYSTEM

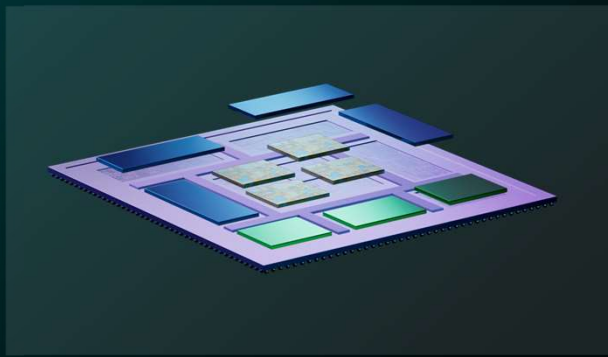
Model-Based Architectural Exploration of Multi-die Systems



Optimize for bandwidth density, energy per bit, cost and latency

Select chip-to-chip protocols and interfaces: UCIe, PCIe, CXL, …

ACCELERATE ARCHITECTURE REALIZATION



Enable silicon, package and software teams with multi-die system analysis

Leverage die-on-die and die-to-die IP models

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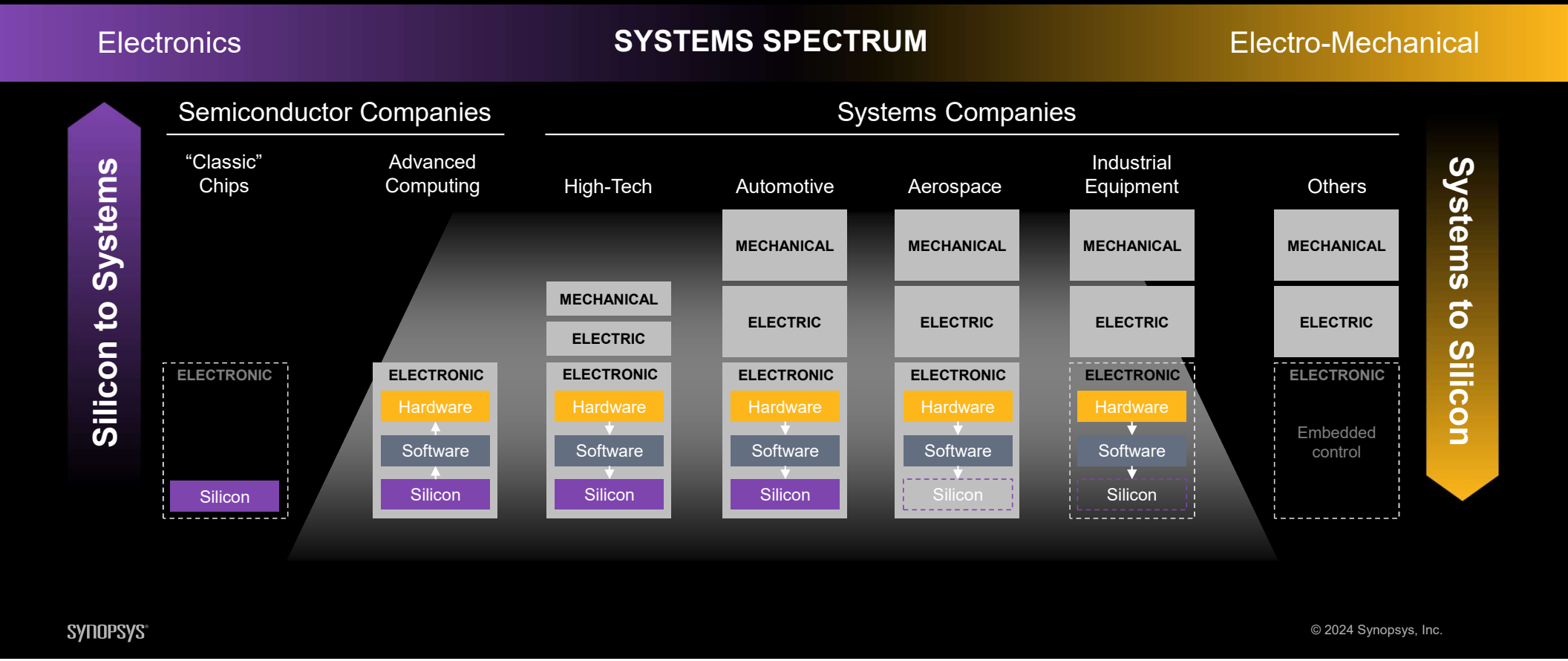
Silicon & System Intersection

Silicon to Systems Transition Ongoing Across Verticals



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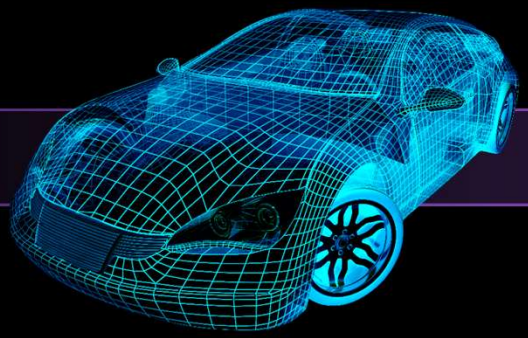
Products Are Becoming SW Platforms In Every Industry

Example: Automotive



Driving Experience → **Digital Platform**

YESTERDAY — TODAY

Automotive Software Market	Lines of Code per Vehicle	Silicon & Software Development Costs	Software as % of Chip Development
2030 **~$84B**	L5 ADAS **~1,000M**	5nm **~$550M**	
~2.5x	**~10x**	**~4x**	**~30-40%**
2020 **~$34B**	Today **100M**	16nm **~$100M**	

Source: Automotive Software and Electronics 2030 (McKinsey, Jul 2019); Levers to Unleash Value (Volkswagen, Jan 2020); Computer on Wheels (Roland Berger, Q1 2020)

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Digital Twins Will Revolutionize CAE for Product Development

Digital Twin

A dynamic virtual model of a physical product

Expected Customer Benefits[1]

Reduce cost of product design and testing	Accelerate product time to market	Improve product quality (HW/SW)	Increase revenue growth & contribution margin
-30%	**+50%**	**+25%**	**~5-10%**
by eliminating physical field test	by testing features before production	by testing HW + SW before production	by reducing costs of physical field testing

Source: Digital twins: The Art of the Possible in Product Development and Beyond (McKinsey, Apr 2022)

1. Percentage increases represent a comparison between without and with digital twin

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Most Comprehensive System Virtualization Solution Portfolio

SYNOPSYS®

Building the Most Comprehensive Digital Twin

Product Operating in Environment *Virtual model of product in environment* Ansys[1]

Virtual Product *Virtual model of product*

Software in Electronics *Software development & test automation* PIKETEC software engineering

INDUSTRY LEADER

Virtualization *Virtual model of chip / ECU* VIRTUALIZER™

INDUSTRY LEADER

Hardware Assisted Verification *Foundational EDA* ZeBu® & HAPS®

2005 2023

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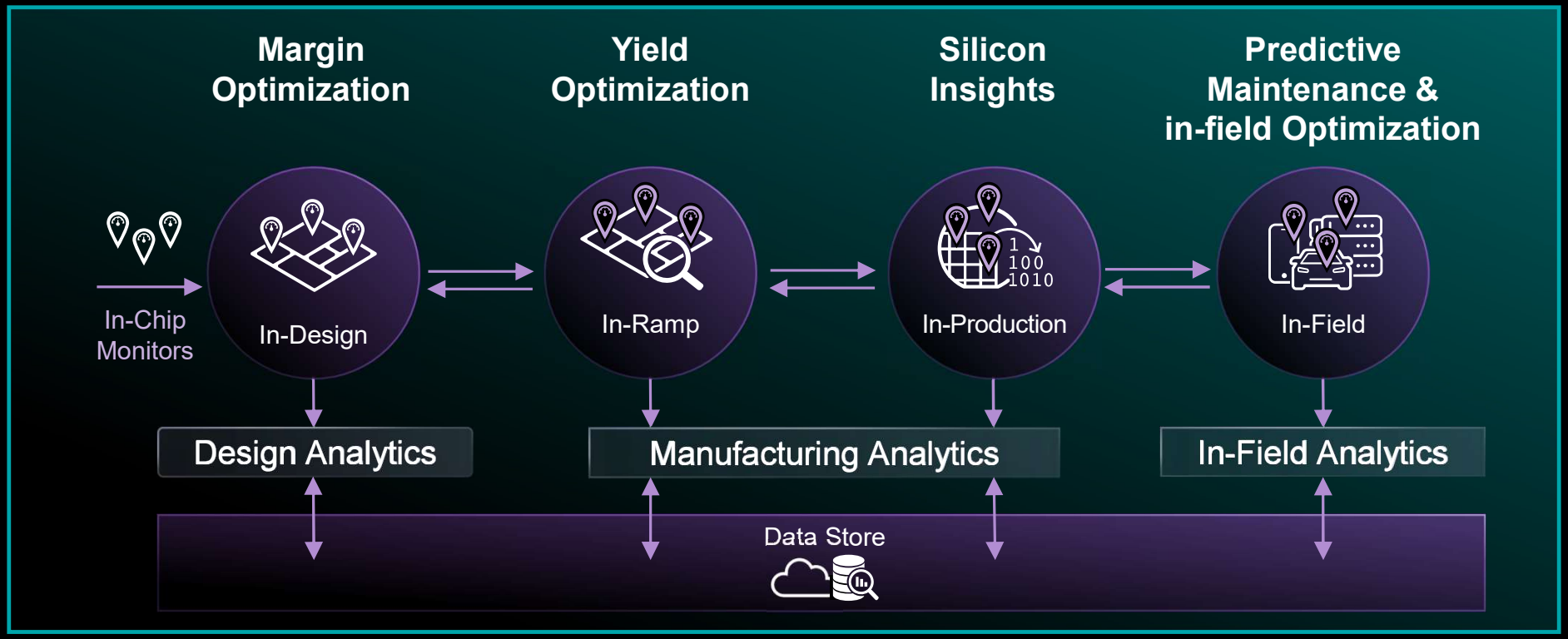
…Including Silicon Lifecycle Management Innovation

Monitoring and optimization of relevant chip metrics across lifecycle stages



Silicon Lifecycle Management

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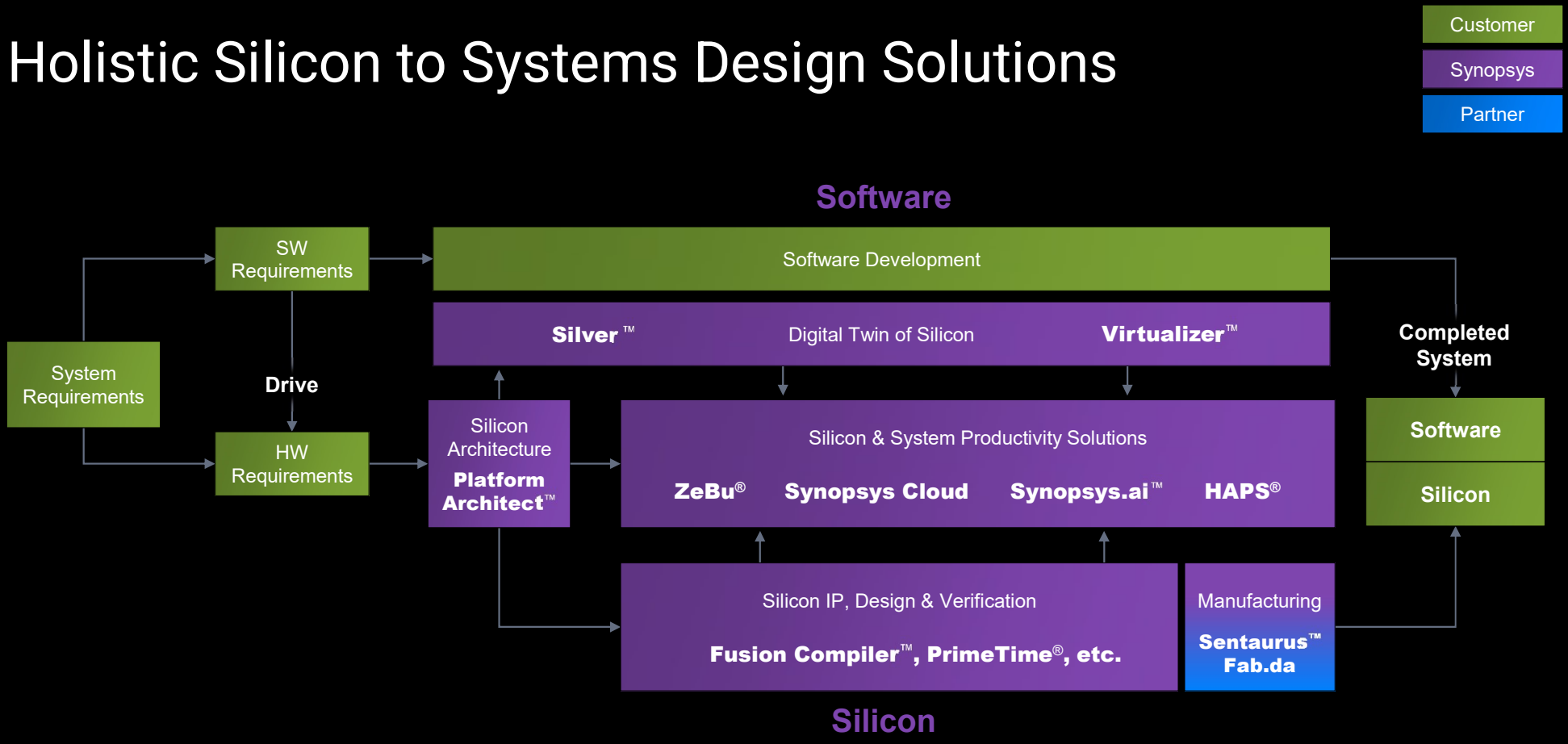
Holistic Silicon to Systems Design Solutions



Addressing complexity and accelerating systems design cycles

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Next-Generation Product Development with Digital Twins

Real world

Product under development

Ansys NVIDIA SYNOPSYS Ansys

Digitized Requirements

External Requirements
Industry Regulations
Internal Requirements

Digital Twin of "World"

Static world models
Dynamic world models
Environment models
Occupant models

Digital Twin of "Physical Product"

Dynamic Models
Sensor models
E/E archtecture models
Chassis models
Powertrain models
Domain models

Digital Twin of Electronics

Digital Twin of Multi-physics

Verification & Validation Environment

NVIDIA Ansys SYNOPSYS

Cloud-based Simulation & Emulation

HiL & ViL

Field Test/ Proving Ground

Product Certification

HiL = Hardware in the Loop
ViL = Vehicle in the Loop

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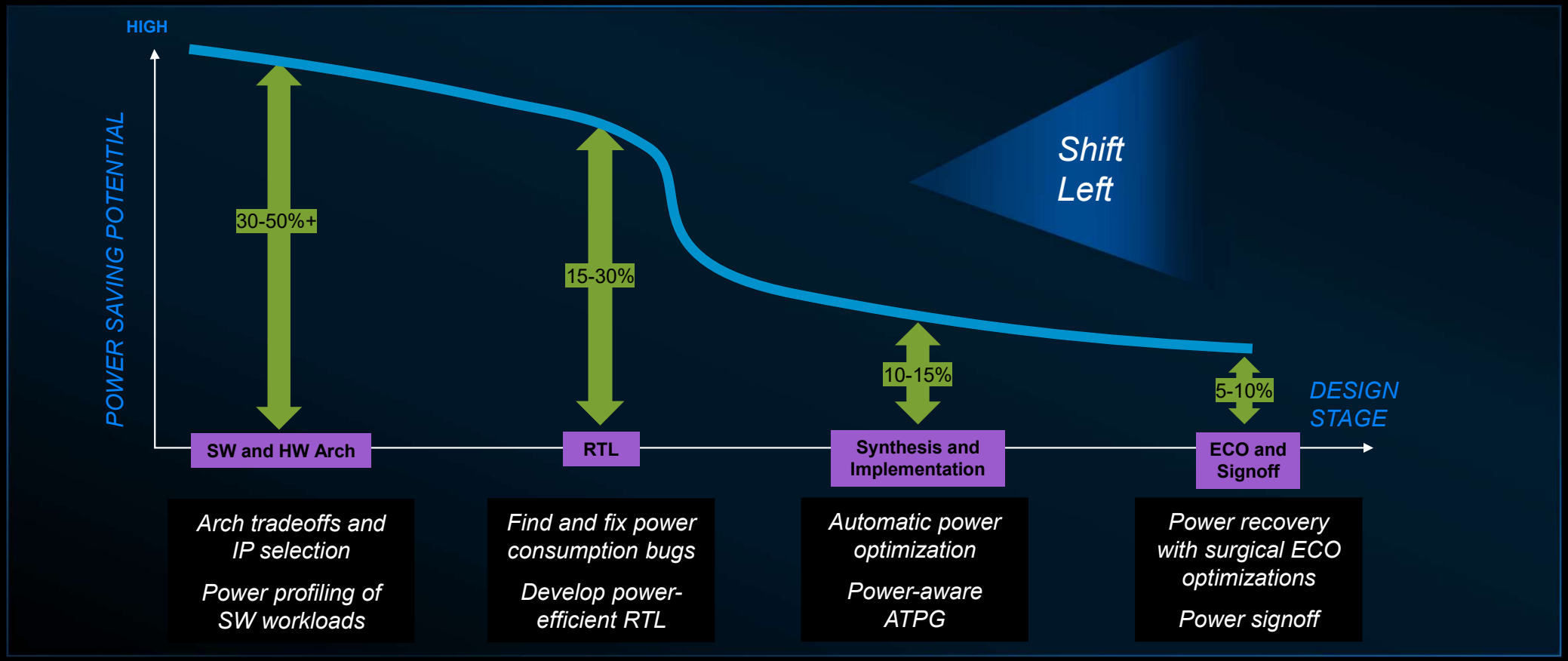
Compute & Energy Limits

Shift-Left Is a Must for Low Power and Energy Efficiency

Bigger opportunity for power savings at earlier design stages



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SLMs a Potential Paradigm Shift in the AI Landscape

LLMs remain for a broader applications, SLMs offer for specialized solutions

	LLM (Large Language Model)	**SLM** (Small Language Model)
Definition	A language model with a very large number of parameters and high complexity.	A language model with fewer parameters and less complexity.
Example	GPT-4	Llama 3 8B, phi-3, Mistral, Gemma
Model Size	GPT-4 around 1.76 trillion parameters	e.g., Llama 3 8B, 8 billion parameters
Application	Ideal for complex applications requiring deep language understanding, generation, and high performance.	Specific tasks and environments, requiring much lesser reasoning and creation, like coding, translation, summarization, etc.
Energy Consumption	Higher energy consumption due to extensive computational requirements and large-scale infrastructure.	Lower energy consumption due to simpler computations and smaller model size.

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Neuromorphic Computing: Supercharged but Energy Efficient

Sequential / Limited Parallel processing	**Operation**	Massively parallel processing
Separated computation and memory	Architecture	Collocated processing and memory
Code as binary instructions	Programming	Spiking neural network
Binary data	Communication	Spikes
Synchronous (Clock-driven)	Timing	Asynchronous (Event-driven)
20 Megawatts (10 exa-FLOPS)	**Energy**	Human Brain 20 Watts (10 exa-FLOPS)

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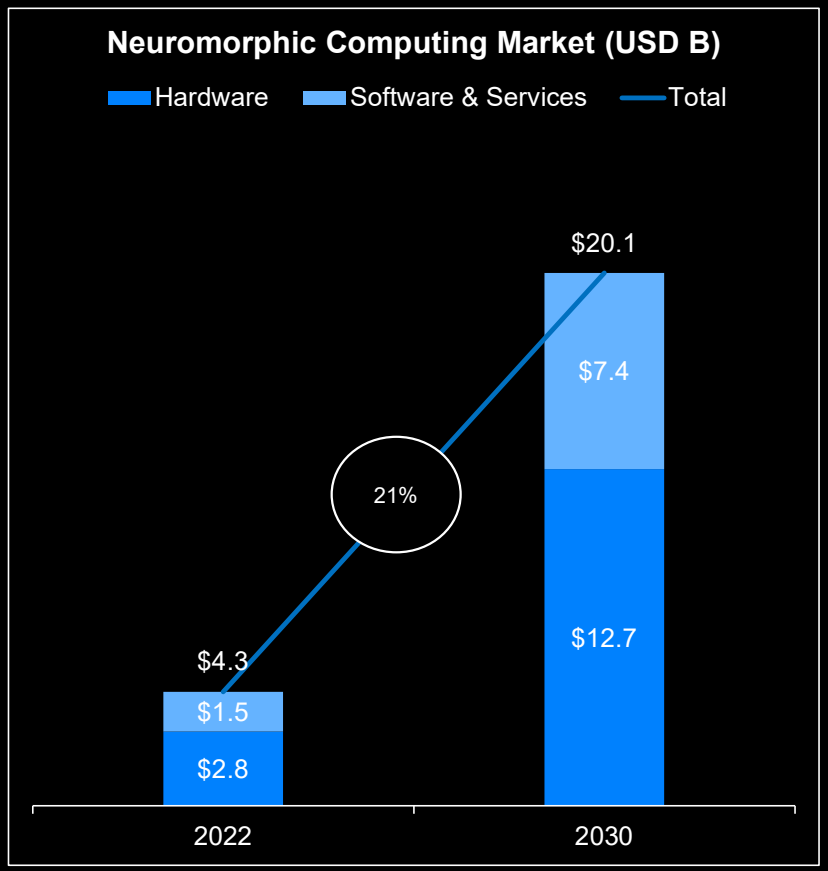
Recent Advances Put Neuromorphic Computing within Reach



✓ Key Movers' Efforts

- Intel has built the world's largest neuromorphic system Hala Point (2024), and utilizes Intel's Loihi 2 processor, which is made using the Intel 4 process and has 128 cores per chip. Each chip includes up to 1 million digital neurons and 120 million synapses.

- IBM's TrueNorth chip has over 1 million neurons and over 256 million synapses. NorthPole (2023) is the next generation of TrueNorth at 12nm

✓ Great Promise to Several Application

Image processing, data processing, and object detection will grow by over 20% CAGR from 2022 to 2030, and penetrate many end markets, such as industrial IoT, automotive, AR/XR, security and surveillance.

✓ Academic Achievements

Carver Mead's pioneering work laid the foundation for brain-inspired systems by demonstrating how silicon circuits could mimic neurobiological processes. Carried forward by his student **Professor Kwabena Boahen**.

✓ Scientific Progress

There are surging neuromorphic patents. 899 patents were granted in 2023. Technical papers significant increased, 8,104 papers were published in 2023.

✓ Government Funding & Project

DARPA SyNAPSE project and the EU Human Brain Project

SYNOPSYS® Source: Polaris Markets

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Neuromorphic Computing Four-Segment Development

	Key Technologies	Key Challenges	Estimated Time to Tech Readiness
SENSING	Neuromorphic sensors In-sensor computing	• Ideal implementation is analog and mixed signal or asynchronous digital designs – challenging to implement at scale	< 3 Years
ALGORITHEM	Computing using Spiking Neural Networks (SNN)	• Training challenges due to limited back propagation • Inefficiency in encoding spikes • Scaling difficult (asynchronous or analog implementation)	> 5 Years
COMPUTING	Neuromorphic Electronics	• Ideal implementation is analog and mixed signal with SNN • Data Communication bottlenecks	> 5 Years
MEMORY	ReRAM	• One-bit to multiple • Shrink down to lower node • High voltage to write	3-5 Years
	MRAM	• Retention failures due to an inherent thermal instability • Manufacturing challenge	
	FeFET	• Short data retention time	>5 Years

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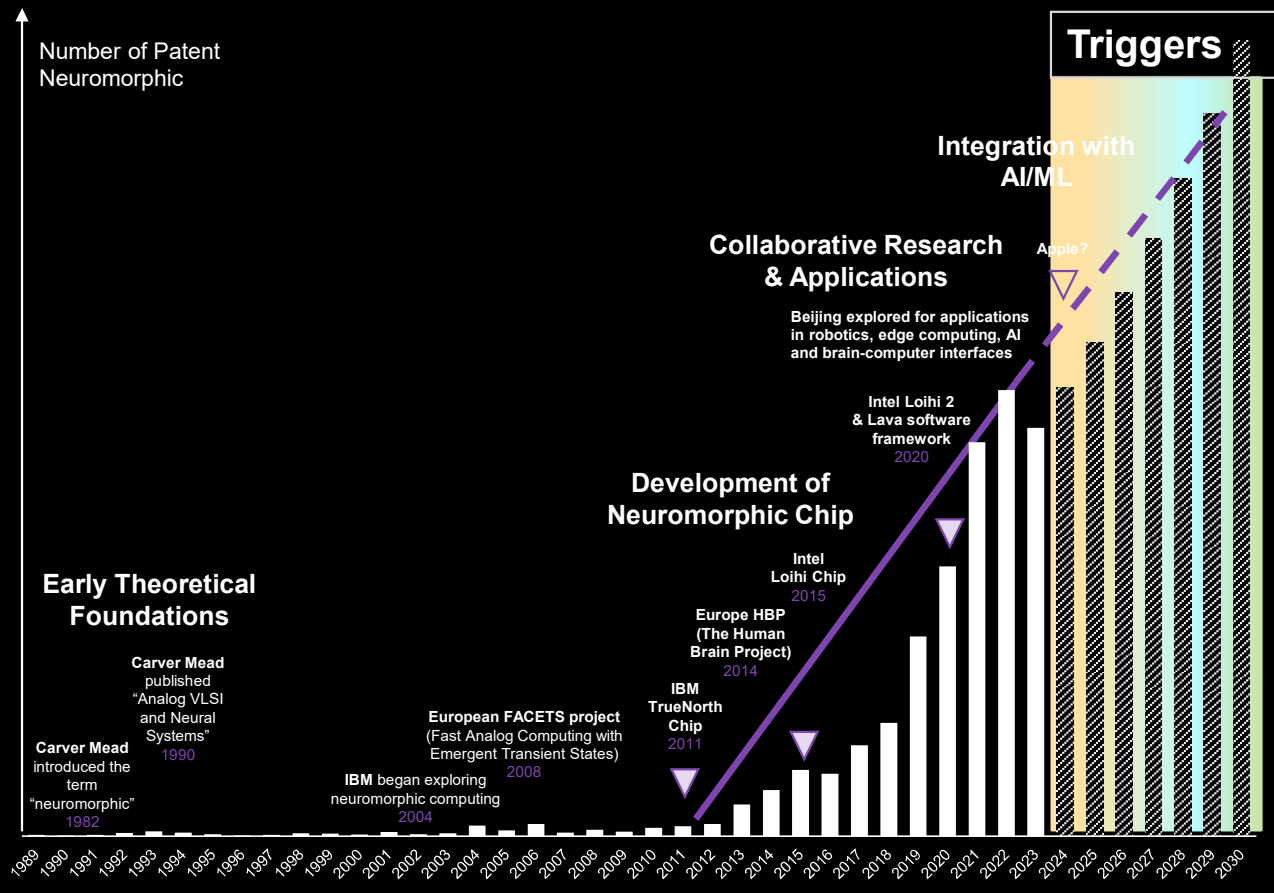
Emerging Memory: The Key to Neuromorphic Computing



Emerging Memory

- Leading process node support below 10nm
- Large Array product Tape out success
- Multi-bit support in memory array

Sensing

- AR/VR headset companies' adoption
- IMC for analog implementation (ideal)

Algorithms

- SNN showing progress beyond current MNIST dataset identification
- IMC at scale

Computing

- Maturity of 3D IC
- Maturity of SNN
- IMC at scale

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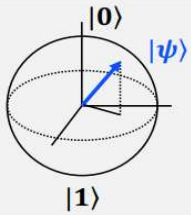
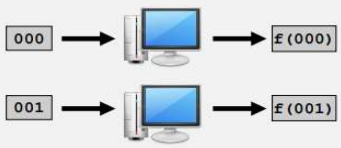
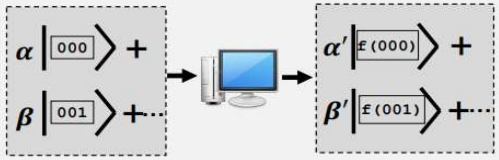
Quantum Leap: Beyond Classical Computing

> "Quantum computers rely on encoding information in a fundamentally different way than classical computers."
>
> –***William Oliver,*** *Director, MIT Center for Quantum Engineering | Professor, MIT EECS*

	Classical Computer	Quantum Computer
Fundamental logic element	**"Bit" : classical bit** (transistor, spin in magnetic memory, …)	**"Qubit" : quantum bit** (any coherent two-level system)
State	**0 "Or" 1**	 **Superposition:** $\alpha\|0\rangle + \beta\|1\rangle$ $\|0\rangle$ **"And"** $\|1\rangle$ $\|\psi\rangle = \alpha\begin{bmatrix}1\\0\end{bmatrix} + \beta\begin{bmatrix}0\\1\end{bmatrix}$
Measurement	• ***Discrete*** **states** • **Deterministic measurement:** Ex: Set as 1, measure as 1	• ***Superposition*** **states** • **Probabilistic measurement:** Ex: If $\|\alpha\| = \|\beta\|$, 50% $\|0\rangle$, 50% $\|1\rangle$
Fundamental logic element	**"Bit" : classical bit** (transistor, spin in magnetic memory, …)	**"Qubit" : quantum bit** (any coherent two-level system)
Computing	• **N bits: One N-bit state** **000, 001, …, 111 (N = 3)** • **Change a bit: new calculation** (classical parallelism) 	• **N qubits: 2^N components to one state** $\alpha\|000\rangle + \beta\|001\rangle + \cdots + \gamma\|111\rangle$ **(N = 3)** • **Quantum parallelism & interference** 

SYNOPSYS® Source: MIT, Qubit Counter

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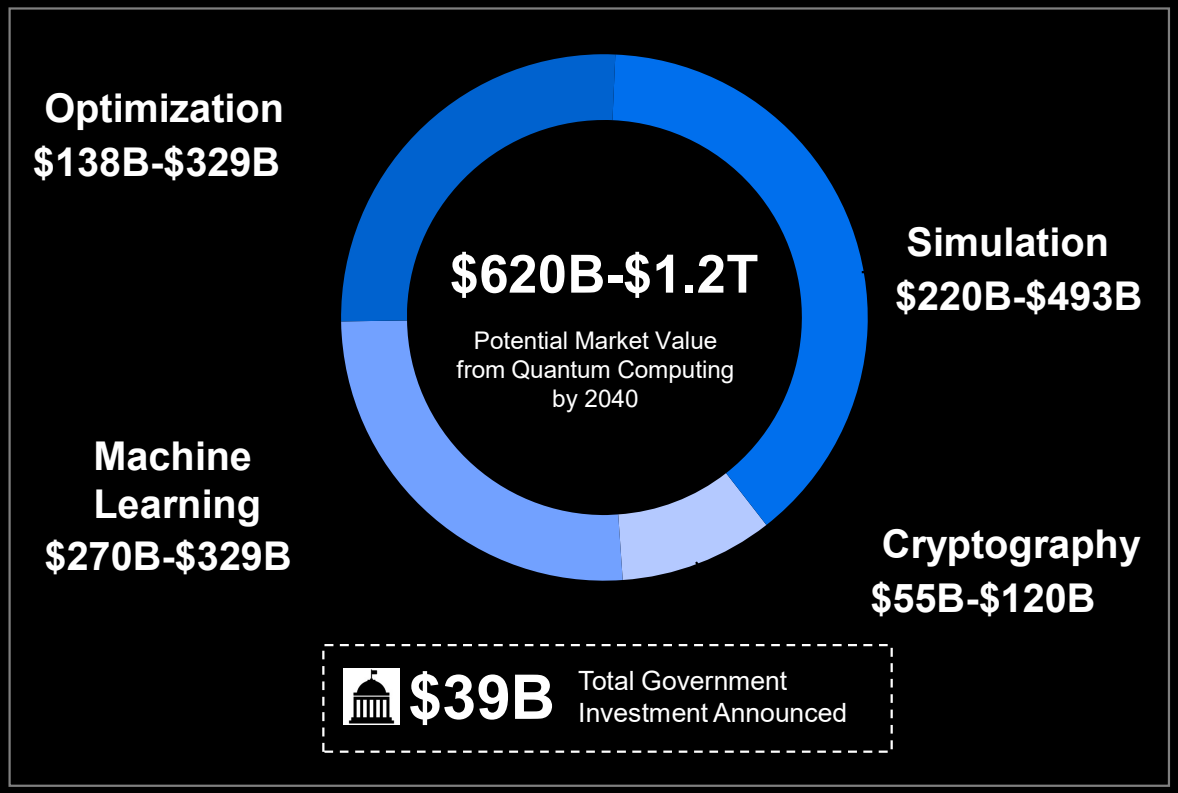
Quantum Computing Development Accelerating



Source: McKinsey, BCG

✓ **Technological Breakthroughs**
IBM unveiled the 1,121 qubits and updated its road map to develop a 4,000+ qubit processor in 2025

✓ **Scientific Progress**
There are surging quantum patents. 16,731 patents were granted in 2023. Quantum papers flat, 111K papers were published in 2023. The papers focus on Quantum Design Automation are on the rise

✓ **Increasing Investment Flows**
More than $5B invested in Quantum Computing by VCs since 2019, equals to above 85% of all VC investments

✓ **Abundant Government Funding**
Governments funding is a major force driving R&D efforts. US has already committed $3.8 billion

✓ **Hyperscalers and Large Semi Companies All-In on Quantum Computing**
Multiple billion dollars are committed by 2029

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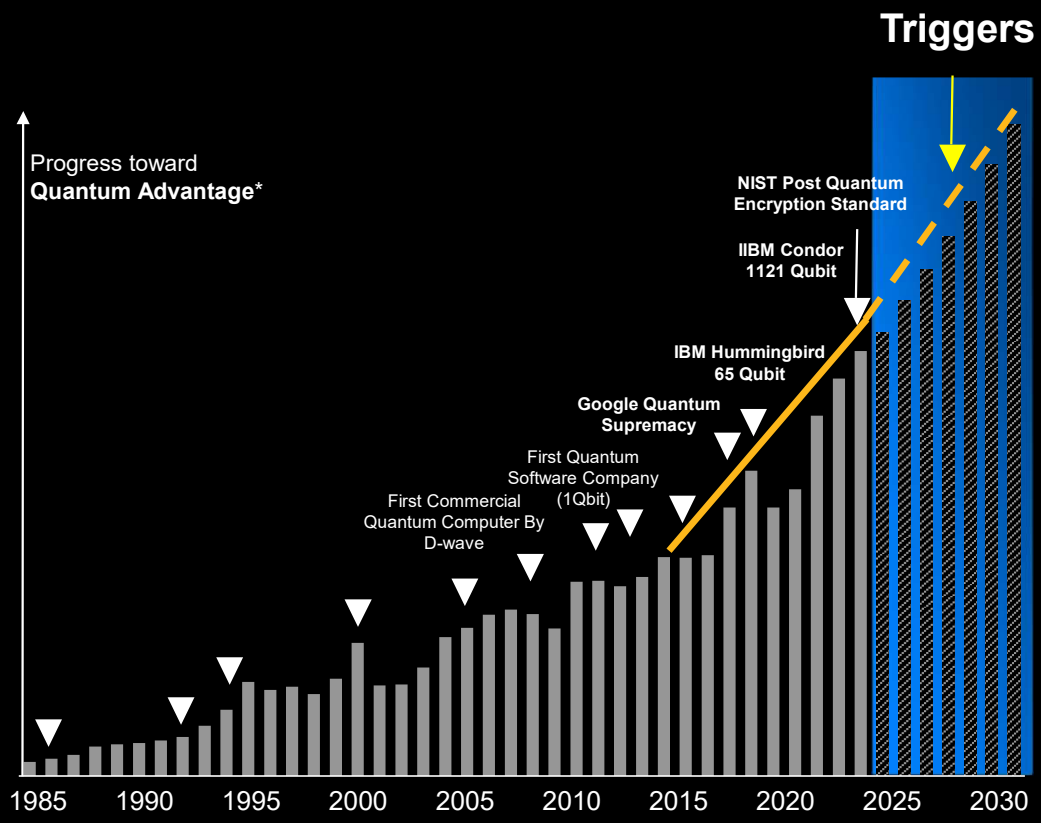
Quantum Takeoff: Potential Ignition Points



- Usage to address substantial real-world problems
- Evident scaling of readout circuit technology, using either multiplexing or optical
- Profitable business model for Quantum Computing presented by a company or partner
- Consistent or reducing energy demand per qubit
- 10:1 error code correction ratio
- Full fault tolerant Quantum computer
- 100,000 qubit quantum computer
- First commercial application

*** Quantum advantage:** refers to the demonstrated and measured success to process a **real-world problem** faster on a quantum computer than on a classical computer

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Quantum Design Automation (QDA) Stack: Navigating Complex Challenges

	Stack	Definition	Key Challenges
QDA	Modeling	Atomistic modeling, parametric extraction, and simulation of quantum devices	Extensive modeling and incorporation of all relevant quantum effects across various operating corners
	Simulation (Emulation)	Replication of quantum behavior for testing and development	Scalability to large numbers of qubits due to limited memory
	Synthesis	Building and optimization of quantum algorithms for specific tasks	Data encoding is expensive Data encoding is also sensitive to noise
	Compilation	Translation of quantum code to run on specific hardware setups	Compilation needs to be hardware aware to choose the implementation that minimizes faults
	Verification/Testing	Confirmation of accuracy and functionality of quantum algorithms and designs	Verifying complex algorithm, such as Harrow-Hassidim-Lloyd algorithm and the Binary Welded Tree quantum walk algorithm, remain difficult
	Schematic Editor/Layout	Creation and modification of quantum circuit designs	Quantum computers haven't reached the scale that necessitates optimized automation solutions
	Error Control	Identification and correction of noise errors in quantum computation processes	Error correction schemes add additional overhead ,but are required to unlock quantum full potential
IP	Control Circuit	Manages quantum processes using CMOS, FPGA, or Josephson junctions for precision control	Implementing Cryo/Cold CMOS at advanced nodes presents significant challenges Lack of a Process Design Kit (PDK) at 22nm poses a constraint to scalability

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Technical Hurdles

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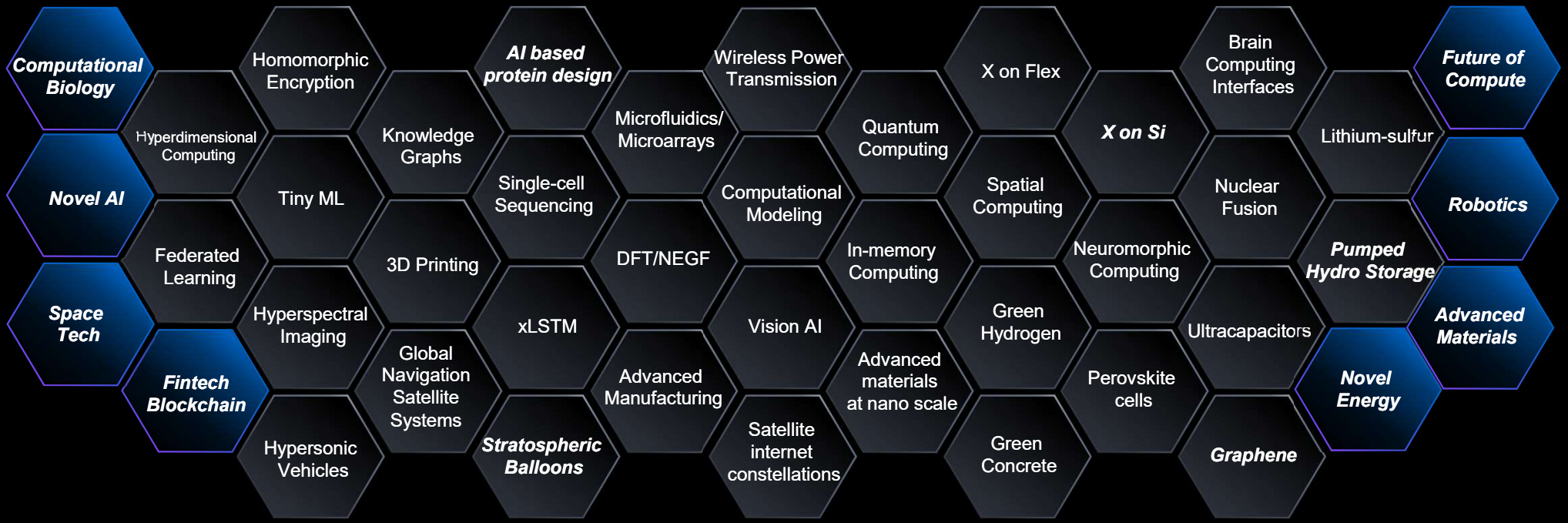

37 Emerging Technologies under 8 Categories

Collaboration, Partnership, Investment

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